Course Code: CSE411	CIE Marks: 60
Course Title: Computer Architecture and Organization	SEE Marks: 40
Credits: 3	

Course Content (from syllabus):

Introduction to computer architecture & organization, Difference between architecture & organization, High-level structures & functions of computers, Evolution of computers Performance evaluation of computing systems, Designing of Computing System, Design methodology, structure Vs Behavior, Different design levels, sequential and combinational circuits, Data representation, combinational logic design, Quine- McCluskey (Q-M) Method-3hours, Processor basics: basic CPU design, Instruction set design, addressing modes, Datapath Design: The Arithmetic and Logic Unit: Integer representation & arithmetic, floating-point representation & arithmetic, Coprocessor, Pipeline processing, Basic structure, Hazards, Branch Prediction, Cache memory overview, Cache mapping, multilevel Cache, unified/split cache, Virtual memory, mapping process, Paging, Demand Paging, Page table, Advantages/ Disadvantages.

Course Description/Rationale:

The computer lies at the heart of computing. Without it most of the computing today would be a branch of theoretical mathematics. To be a professional in any field of computing today, one should not regard the computer as just a black box that executes programs by magic. All students of computing should acquire some understanding and appreciation of a computer system's functional components, their characteristics, their performance, and their interactions. This course can help the students in this regard.

Course Objective

To provide fundamental and conceptual knowledge of structure, behavior and characteristics of the computer system and computing. Precisely:

- To learn the basic concepts of architecture & organization.
- To learn the performance evaluation of computing systems.
- To learn about the designing of Computing System.
- To learn about sequential and combinational circuit design.
- To learn the basic of CPU, instruction set, addressing modes, and Datapath design.
- To learn about pipeline processing and different types of hazards.
- To learn details about case and virtual memory mapping.

Course Learning Outcome (CLO): (at the end of the course, student will be able to do:)

CLO1	**Define** the functional components in processor design, computer arithmetic, instruction code, and addressing modes.
CLO2	**Summarized** factors in the processor design to achieve performance in single and multiprocessing systems.
CLO3	**Identify** the operations of cache and main memory, I/O operations, characteristics, bus controls to design a computer system.
CLO4	C**onstruct** specification of a typical computer system with the knowledge of system components like cache and virtual memory.

Content of the course:

SL	Course Content (as summary)	Hrs.	CLO's
1.	Introduction: to computer architecture & organization	1.5 Hours	CLO-1
2.	Difference between architecture & organization	1.5 Hours	CLO-1
3.	High-level structures & functions of computers	1.5 Hours	CLO-1
4.	Evolution of computers	1.5 Hours	CLO-2
5.	Performance evaluation of computing systems	1.5 Hours	CLO-2
6.	Designing of Computing System	1.5 Hours	CLO-2
7.	Design methodology, structure Vs Behavior	1.5 Hours	CLO-2
8.	Different design levels, sequential and combinational circuits	1.5 Hours	CLO-2
9.	Data representation, combinational logic design	1.5 Hours	CLO-3
10.	Quine- McCluskey (Q-M) Method-3hours	1.5 Hours	CLO-3
11.	Processor basics: basic CPU design	1.5 Hours	CLO-3
12.	Instruction set design, addressing modes	1.5 Hours	CLO-3
13.	Datapath Design: The Arithmetic and Logic Unit: Integer representation & arithmetic	1.5 Hours	CLO-3
14.	Floating-point representation & arithmetic, Coprocessor.	1.5 Hours	CLO-4
15.	Pipeline processing, Basic structure	1.5 Hours	CLO-4
16.	Hazards, Branch Prediction.	1.5 Hours	CLO-4
17.	Cache memory overview, Cache mapping	1.5 Hours	CLO-4
18.	Multilevel Cache, unified/split cache.	1.5 Hours	CLO-4
19.	Virtual memory, mapping process	1.5 Hours	CLO-4
20.	Paging, Demand Paging, Page table, Advantages/ Disadvantages.	1.5 Hours	CLO-4

Mapping of Course Learning Outcomes to Program Learning Outcomes

	PLO-1	PLO-2	PLO-3	PLO-4	PLO-5	PLO-6	PLO-7	PLO-8	PLO-9	PLO-10	PLO-11	PLO-12
CLO1	√											
CLO2		√										
CLO3			√									
CLO4				√								

Mapping Course Learning Outcome (CLOs) with the Teaching-Learning and Assessment Strategy:

CLO's	Teaching Learning Strategy	Assessment Strategy	Corresponding PLO number	Domain Level/Learning Taxonomy
CLO1	Identify the basics organization of a computing system, find out the differentiate between the concept of architecture and organization, and can perform the evaluation the true performance of a computer for the enhancements of computer performance.	Quiz/Assignment	PLO1	L1
CLO2	Students will be able to understand how computer represent different types of data and will able to learn how basic elements of a computer works with different level of processor design. Also learn about basic CPU design, instruction set design, addressing modes	Midterm/Quiz	PLO2	L2
CLO3	Realized the Arithmetic and Logic Unit, Integer representation & arithmetic, floating-point representation & arithmetic, Coprocessor. Also understand Pipeline processing, Basic structure, Hazards, Branch Prediction.	Midterm/Final/Quiz	PLO3	L3
CLO4	Understand the concept of cache mapping, multilevel Cache, unified/split cache. And realized virtual memory, mapping process, Paging, Demand Paging, Page table.	Final/Quiz/Presentation	PLO4	L4

Course Delivery Plan/Lesson Delivery Plan:

Week/Lessen (hour)	Discussion Topic & Book Reference	Student Activities during Online and Onsite and TLA	Mapping with CLO and PLO	Assessment Plan
Week 1 Lessen 1 & 2 [3 Hours]	**Lesson 1:** Introduction to Computer Organization and Architecture. (Ref. Text Jhon P. Hayes: Ch 1)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1**	CLO1, CLO2/PLO 1, PLO2	
	Lesson 2: Discuss the basic concepts and structure of computers. (Ref. Text Jhon P. Hayes: Ch 1)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA2**		
Week 2 Lessen 3 & 4 [3 Hours]	**Lesson 3:** History of computing. (Ref. Text Jhon P. Hayes: Ch 1)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1**	CLO1, CLO2/PLO 1, PLO2	
	Lesson 4: Comparison between electrical and mechanical computers and summarize the functional units of computer. (Ref. Text Jhon P. Hayes: Ch 1)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA3**		
Week 3 Lessen 5 & 6 [3 Hours]	**Lesson 5:** Evolution of computers. (Ref. Text Jhon P. Hayes: Ch 1)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1**	CLO1, CLO2/PL1, PLO2	**Class Test# 1** Either online/onsite based on Week-1 and Week -2 discussion.
	Lesson 6: Performance evaluation of computing systems. (Ref. Text Jhon P. Hayes: Ch 1)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; TLA1, TLA2, TLA3, TLA4		

Week 4 Lessen 7 & 8 [3 Hours]	**Lesson 7: C**ontinued and understanding performance. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA2, TLA3**	CLO2/PL2	**Assignment-1** [will be due by week 6] Topic: Performance evaluation
	Lesson 8: System representation and design process. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA2**		
Week 5 Lessen 9 & 10 [3 Hours]	**Lesson 9:** Register and gate level design. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA3, TLA4**	CLO1, CLO2/PL1, PLO2	**Class Test# 2** Either online/onsite based on Week-4 and Week -5 discussion.
	Lesson 10: Understand concepts of register transfer logic and types of micro-operations. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; TLA**1, TLA3, TLA4**		
Week 6 Lessen 11 & 12 [3 Hours]	**Lesson 11:** Processor level design and design logic circuits for different micro-operations. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA2**	CLO1, CLO3/PLO1, PLO2	Student Submit Assigment-1 in BLC (online) or hard copy
	Lesson 12: Data representation and encoding. (Ref. Text: John P. Hayes	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; **TLA1, TLA2**		
Week 7 Lessen 13 & 14 [3 Hours]	**Lesson 13:** Sequential and Combinational logic design (Ref. Text: John P. Hayes Ch 3.2)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; **TLA1, TLA2**	CLO3/PLO2	**Assignment-2** Topic: Datapath Design

	Lesson 14: Quine- McCluskey (Q-M) Method-3hours (Ref. Text: John P. Hayes Ch 3.2)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; **TLA1, TLA2**	CLO3/PLO 2	
Week 8 Lessen 15 & 16 [3 Hours]	**Lesson 15:** Instruction set characteristics and types of instruction formats. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA3**	CLO3/PLO 2	
	Lesson 16: Basic CPU design. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA3**		
Week 9	**Midterm Examination** **Syllabus: Week 1 – Week 8**			
Week 10 Lessen 17 & 18 [3 Hours]	**Lesson 17:** Datapath Design: The Arithmetic and Logic Unit: Integer representation & arithmetic (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA3**	CLO3 /PL2	**<u>Assignment-3</u>** [will be due by week-14] Topic: Addressing Modes
	Lesson 18: floating-point representation & arithmetic, Coprocessor. (Ref. Text: John P. Hayes)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA3**		
Week 11 Lessen 19 & 20 [3 Hours]	**Lesson 19:** Addressing modes, Data Transfer and manipulations. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1, TLA2**	CLO3/P L2	
	Lesson 20: Asynchronous data transfer, Modes of Transfer and RISC, CISC. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TAL1, TLA3**		
Week 12 Lessen 21 & 22 [3 Hours]	**Lesson 21:** Pipelining strategy, performance. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; **TLA1**	CLO1, CLO4/P L1, PLO3, PLO4	

	Lesson 22: Pipeline hazards and measures against pipeline hazards. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; **TLA1, TLA2, TLA4**		
Week 13 Lessen 23 & 24 [3 Hours]	**Lesson 23:** Arithmetic pipeline, Instruction pipeline, RISC Pipeline. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; **TLA1, TLA2**	CLO3, CLO4/ PLO2, PLO3, PLO4	
	Lesson 24: Memory hierarchy and introduction to cache memory. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g., Voice over PPT, PPT, Video, H5P; **TLA1**		
Week 14 Lessen 25 & 26 [3 Hours]	**Lesson 25:** Cache addressing and cache mapping functions. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, PPT, Video, H5P; **TLA1, TLA3**	CLO4/PL3, PLO4	**Class Test# 3** Either online/onsite based on Week-11 and Week -12 discussion.
	Lesson 26: Direct memory addressing or cache mapping functions (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, PPT, Video, H5P; **TLA1, TLA3**		
Week 15 Lessen 27 & 28 [3 Hours]	**Lesson 27:** Associative and Set-Associative memory addressing or cache mapping functions (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, PPT, Video, H5P; **TLA1, TLA3**	CLO4/PL4, PLO4	Student Submit Assigment-3 in BLC (online) or hard copy
	Lesson 28: Introduction to Virtual memory and memory mapping technique. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, PPT, Video, H5P; TLA4		
Week 16 Lessen 29 & 30 [3 Hours]	**Lesson 29:** Demand Paging. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, PPT, Video, H5P; TLA3, TLA4	CLO4/PLO3, PLO4	**Presentation** based on the discussion of Week- 15 and 16

	Lesson 30: Page table, Advantages/ Disadvantages. (Ref. Text: W. Stallings)	Online/Onsite discussion; Review Feedback online; Using Interactive content e.g. Voice over PPT, P P T , Video, H5P; TLA3, TLA4		
Week 17 Lessen 31 & 32 [3 Hours]	**Lesson 31:** Review class	TLA3, TLA4		
	Lesson 32: Review class	TLA3, TLA4		
Week 18	**Final Examination Syllabus: Week 10 – Week 17**			

Assessment Pattern:

Assessment Task	**CO's**					**Mark (Total=100)**
	CO1	**CO2**	**CO3**	**CO4**	**CO5**	
Attendance	--	--	--	--	--	7
Class Test (CT1, CT2, CT3)	--	--	--	--	--	15
Assignment	--	--	--	--	--	5
Presentation	--	--	--	--	--	8
Midterm Examination	5	10	10	0	--	25
Semester Final Examination	0	10	10	20	--	40
Total Mark	5	20	20	20	--	100

CIE – Breakup (Theory) [60 marks]

Bloom's Criteria	**Attendance (07)**	**Class Test (15)**	**Assignment (05)**	**Presentation (08)**	**Mid Exam (25)**
Remember		05			05
Understand		05	02	02	10
Apply		05		03	05
Analyze			03		05
Evaluate					00
Create				03	00

SEE – Semester End Examination [40 marks] {Theory}

Bloom Criteria	Score for the Test
Remember	05
Understand	10
Apply	15
Analyze	05
Evaluate	05
Create	00

Learning Materials:

Textbook/Recommended Readings:

1. Computer Organization and Architecture, Author: William Stallings, 9th edition
2. Computer Architecture and Organization, Author: John P. Hayes, Third Edition

Reference Books/Supplementary Readings:

1. Computer Architecture- A Quantitative Approach, by David A. Patterson and John L. Hennessy, 4th edition.
2. Fundamentals of Digital Logic with Verilog Design by Stephen Brown & Zvonko Vranesic.
3. Microprocessors and Microcomputer-Based System Design by Mohamed Rafiquzzaman.

Other Readings:

1. Form BLC Course Blog
2. Different supporting tutorials from YouTube