Contents

5 Semiconductor Physics

INTRODUCTION

Certain substances like germanium, silicon, carbon etc. are neither good conductors like copper nor insulators like glass. In other words, the resistivity of these materials lies inbetween conductors and insulators. Such substances are classified as *semiconductors.* Semiconductors have some useful properties and are being extensively used in electronic circuits. For instance, *transistor*—a semiconductor device is fast replacing bulky vacuum tubes in almost all applications. Transistors are only one of the family of semiconductor devices ; many other semiconductor devices are becoming increasingly popular. In this chapter, we shall focus our attention on the different aspects of semiconductors.

5.1 Semiconductor

It is not easy to define a semiconductor if we want to take into account all its physical characteristics. However, generally, a semiconductor is defined on the basis of electrical conductivity as under :

A **semiconductor** *is a substance which has resistivity (10^{-4} to 0.5 Ωm) inbetween conductors and insulators e.g. germanium, silicon, selenium, carbon etc.*

The reader may wonder, when a semiconductor is neither a good conductor nor an insulator, then why not to classify it as a *resistance material* ? The answer shall be readily available if we study the following table :

S.No.	Substance	Nature	Resistivity
1	Copper	good conductor	1.7×10^{-8} Ω m
2	Germanium	semiconductor	0.6 Ω m
3	Glass	insulator	9×10^{11} Ω m
4	Nichrome	resistance material	10^{-4} Ω m

Comparing the resistivities of above materials, it is apparent that the resistivity of germanium (semiconductor) is quite high as compared to copper (conductor) but it is quite low when compared with glass (insulator). This shows that resistivity of a semiconductor lies inbetween conductors and insulators. However, it will be wrong to consider the semiconductor as a resistance material. For example, nichrome, which is one of the highest resistance material, has resistivity much lower than germanium. This shows that electrically germanium cannot be regarded as a conductor or insulator or a resistance material. This gave such substances like germanium the name of semiconductors.

It is interesting to note that it is not the resistivity alone that decides whether a substance is semiconductor or not. For example, it is just possible to prepare an alloy whose resistivity falls within the range of semiconductors but the alloy cannot be regarded as a semiconductor. In fact, semiconductors have a number of peculiar properties which distinguish them from conductors, insulators and resistance materials.

Properties of Semiconductors

(*i*) The resistivity of a semiconductor is less than an insulator but more than a conductor.

(*ii*) Semiconductors have *negative temperature co-efficient of resistance* *i.e.* the resistance of a semiconductor decreases with the increase in temperature and *vice-versa*. For example, germanium is actually an insulator at low temperatures but it becomes a good conductor at high temperatures.

(*iii*) When a suitable metallic impurity (*e.g.* arsenic, gallium etc.) is added to a semiconductor, its current conducting properties change appreciably. This property is most important and is discussed later in detail.

5.2 Bonds in Semiconductors

The atoms of every element are held together by the bonding action of valence electrons. This bonding is due to the fact that it is the tendency of each atom to complete its last orbit by acquiring 8 electrons in it. However, in most of the substances, the last orbit is incomplete *i.e.* the last orbit does not have 8 electrons. This makes the atom active to enter into bargain with other atoms to acquire 8 electrons in the last orbit. To do so, the atom may lose, gain or share valence electrons with other atoms. In semiconductors, bonds are formed by sharing of valence electrons. Such bonds are called *co-valent bonds*. In the formation of a co-valent bond, each atom contributes equal number of valence electrons and the contributed electrons are shared by the atoms engaged in the formation of the bond.

Fig. 5.1 shows the co-valent bonds among germanium atoms. A germanium atom has *4 valence electrons. It is the tendency of each germanium atom to have 8 electrons in the last orbit. To do so, each germanium atom positions itself between four other germanium atoms as shown in Fig. 5.1 (*i*). Each neighbouring atom shares one valence electron with the central atom. In this business of sharing, the central atom completes its last orbit by having 8 electrons revolving around the nucleus. In this way, the central atom sets up co-valent bonds. Fig. 5.1 (*ii*) shows the bonding diagram.

The following points may be noted regarding the co-valent bonds :

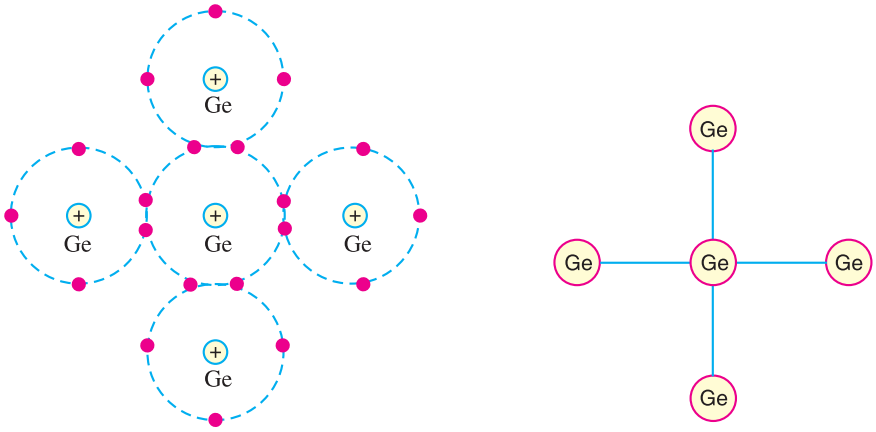
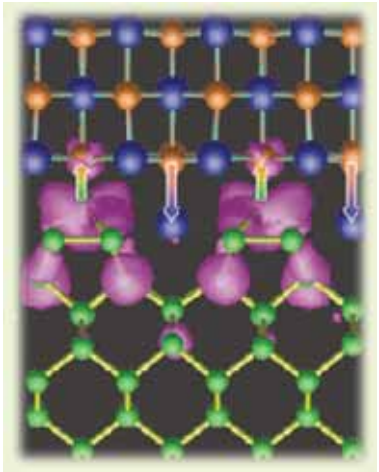


Fig. 5.1

(*i*) Co-valent bonds are formed by sharing of valence electrons.

(*ii*) In the formation of co-valent bond, each valence electron of an atom forms direct bond with the valence electron of an adjacent atom. In other words, valence electrons are associated with particular atoms. For this reason, valence electrons in a semiconductor are not free.



Bonds in Semiconductor

5.3 Crystals

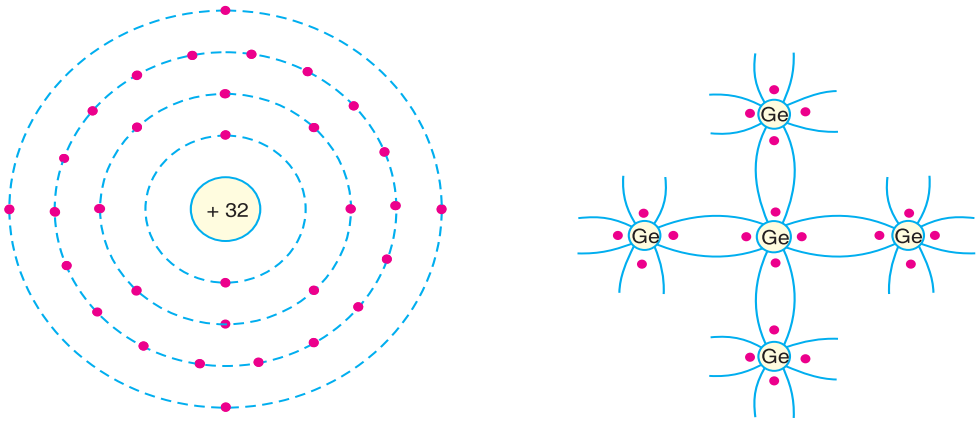
A substance in which the atoms or molecules are arranged in an orderly pattern is known as a *crystal*. All semi-conductors have crystalline structure. For example, referring to Fig. 5.1, it is clear that each atom is surrounded by neighbouring atoms in a repetitive manner. Therefore, a piece of germanium is generally called germanium crystal.

5.4 Commonly Used Semiconductors

There are many semiconductors available, but very few of them have a practical application in electronics. The two most frequently used materials are *germanium* (Ge) and *silicon* (Si). It is because the energy required to break their co-valent bonds (*i.e.* energy required to release an electron from their valence bands) is very small; being about 0.7 eV for germanium and about 1.1 eV for silicon. Therefore, we shall discuss these two semiconductors in detail.

* A germanium atom has 32 electrons. First orbit has 2 electrons, second 8 electrons, third 18 electrons and the fourth orbit has 4 electrons.

(*i*) Germanium. Germanium has become the model substance among the semiconductors; the main reason being that it can be purified relatively well and crystallised easily. Germanium is an earth element and was discovered in 1886. It is recovered from the ash of certain coals or from the flue dust of zinc smelters. Generally, recovered germanium is in the form of germanium dioxide powder which is then reduced to pure germanium.

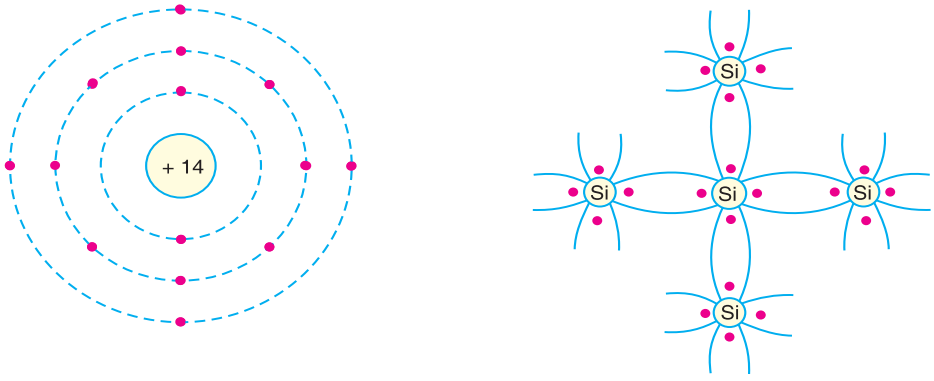


(*i*) (*ii*)

Fig. 5.2

The atomic number of germanium is 32. Therefore, it has 32 protons and 32 electrons. Two electrons are in the first orbit, eight electrons in the second, eighteen electrons in the third and four electrons in the outer or valence orbit [See Fig. 5.2 (*i*)]. It is clear that germanium atom has four valence electrons *i.e.*, it is a tetravalent element. Fig. 5.2 (*ii*) shows how the various germanium atoms are held through co-valent bonds. As the atoms are arranged in an orderly pattern, therefore, germanium has crystalline structure.

(*ii*) Silicon. Silicon is an element in most of the common rocks. Actually, sand is silicon dioxide. The silicon compounds are chemically reduced to silicon which is 100% pure for use as a semiconductor.



(*i*) (*ii*)

Fig. 5.3

The atomic number of silicon is 14. Therefore, it has 14 protons and 14 electrons. Two electrons are in the first orbit, eight electrons in the second orbit and four electrons in the third orbit [See Fig. 5.3 (*i*)]. It is clear that silicon atom has four valence electrons *i.e.* it is a tetravalent element. Fig. 5.3 (*ii*) shows how various silicon atoms are held through co-valent bonds. Like germanium, silicon atoms are also arranged in an orderly manner. Therefore, silicon has crystalline structure.

5.5 Energy Band Description of Semiconductors

It has already been discussed that a semiconductor is a substance whose resistivity lies between conductors and insulators. The resistivity is of the order of 10^{-4} to 0.5 ohm metre. However, a semiconductor can be defined much more comprehensively on the basis of energy bands as under :

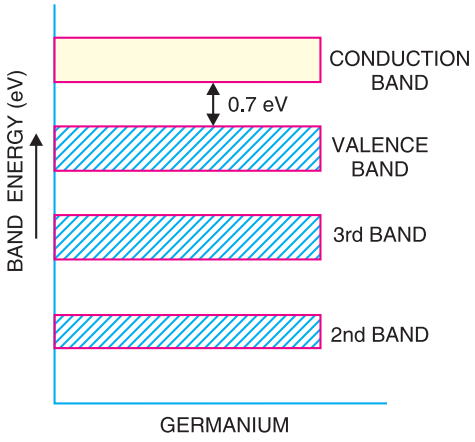


Fig. 5.4

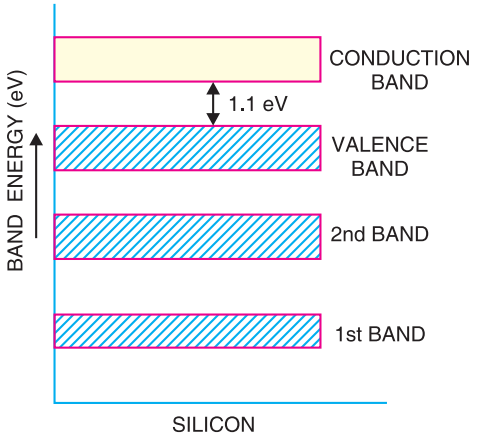


Fig. 5.5

A **semiconductor** *is a substance which has almost filled valence band and nearly empty conduction band with a very small energy gap (≃ 1 eV) separating the two.*

Figs. 5.4 and 5.5 show the energy band diagrams of germanium and silicon respectively. It may be seen that forbidden energy gap is very small; being 1.1 eV for silicon and 0.7 eV for germanium. Therefore, relatively small energy is needed by their valence electrons to cross over to the conduction band. Even at room temperature, some of the valence electrons may acquire sufficient energy to enter into the conduction band and thus become free electrons. However, at this temperature, the number of free electrons available is very *small. Therefore, at room temperature, a piece of germanium or silicon is neither a good conductor nor an insulator. For this reason, such substances are called *semiconductors.*

The energy band description is extremely helpful in understanding the current flow through a semiconductor. Therefore, we shall frequently use this concept in our further discussion.

5.6 Effect of Temperature on Semiconductors

The electrical conductivity of a semiconductor changes appreciably with temperature variations. This is a very important point to keep in mind.

(*i*) At absolute zero. At absolute zero temperature, all the electrons are tightly held by the semiconductor atoms. The inner orbit electrons are bound whereas the valence electrons are engaged in co-valent bonding. At this temperature, the co-valent bonds are very strong and there are no free electrons. Therefore, the semiconductor crystal behaves as a perfect insulator [See Fig. 5.6 (*i*)].

In terms of energy band description, the valence band is filled and there is a large energy gap between valence band and conduction band. Therefore, no valence electron can reach the conduction band to become free electron. It is due to the non-availability of free electrons that a semiconductor behaves as an insulator.

* Out of 10^{10} semiconductor atoms, one atom provides a free electron.

(*ii*) Above absolute zero. When the temperature is raised, some of the covalent bonds in the semiconductor break due to the thermal energy supplied. The breaking of bonds sets those electrons *free* which are engaged in the formation of these bonds. The result is that a few free electrons exist in the semiconductor. These free electrons can constitute a tiny electric current if potential difference is

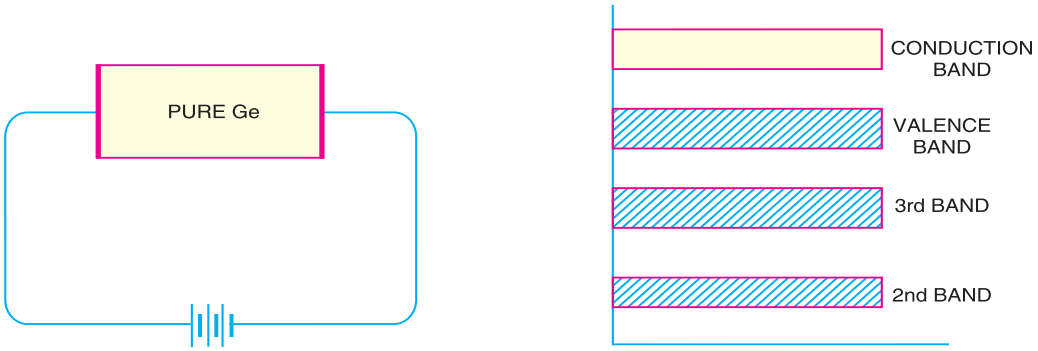


Fig. 5.6

applied across the semiconductor crystal [See Fig. 5.7 (*i*)]. *This shows that the resistance of a semiconductor decreases with the rise in temperature i.e.* it has negative temperature coefficient of resistance. It may be added that at room temperature, current through a semiconductor is too small to be of any practical value.

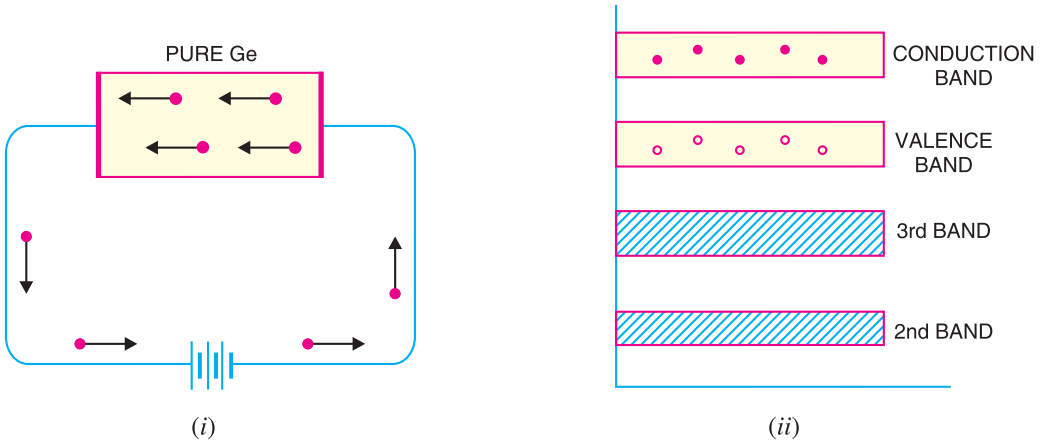


Fig. 5.7

Fig. 5.7 (*ii*) shows the energy band diagram. As the temperature is raised, some of the valence electrons acquire sufficient energy to enter into the conduction band and thus become free electrons. Under the influence of electric field, these free electrons will constitute electric current. It may be noted that each time a valence electron enters into the conduction band, a *hole* is created in the valence band. As we shall see in the next article, holes also contribute to current. In fact, hole current is the most significant concept in semiconductors.

5.7 Hole Current

At room temperature, some of the co-valent bonds in pure semiconductor break, setting up free electrons. Under the influence of electric field, these free electrons constitute electric current. At the

same time, another current – the hole current – also flows in the semiconductor. When a covalent bond is broken due to thermal energy, the removal of one electron leaves a vacancy *i.e.* a missing electron in the covalent bond. This missing electron is called a *hole which acts as a positive charge. For one electron set free, one hole is created. Therefore, thermal energy creates *hole-electron pairs*; there being as many holes as the free electrons. The current conduction by holes can be explained as follows :

The hole shows a missing electron. Suppose the valence electron at *L* (See Fig. 5.8) has become free electron due to thermal energy. This creates a hole in the co-valent bond at *L*. The hole is a strong centre of attraction **for the electron. A valence electron (say at *M*) from nearby co-valent bond comes to fill in the hole at *L*. This results in the creation of hole at *M*. Another valence electron (say at *N*) in turn may leave its bond to fill the hole at *M*, thus creating a hole at *N*. Thus the hole having a positive charge has moved from *L* to *N i.e.* towards the negative terminal of supply. This constitutes *hole current*.

It may be noted that hole current is due to the movement of ***valence electrons from one co-valent bond to another bond. The reader may wonder why to call it a hole current when the conduction is again by electrons (of course *valence electrons* !). The answer is that the basic reason for current flow is the presence of holes in the co-valent bonds. Therefore, it is more appropriate to consider the current as the movement of holes.

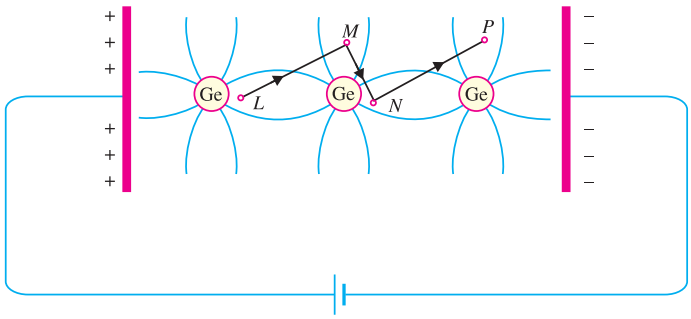


Fig. 5.8

Energy band description. The hole current can be beautifully explained in terms of energy bands. Suppose due to thermal energy, an electron leaves the valence band to enter into the conduction band as shown in Fig. 5.9.

This leaves a vacancy at *L*. Now the valence electron at *M* comes to fill the hole at *L*. The result is that hole disappears at *L* and appears at *M*. Next, the valence electron at *N* moves into the hole at *M*. Consequently, hole is created at *N*. It is clear that valence electrons move along the path *PNML* whereas holes move in the opposite direction *i.e.* along the path *LMNP*.

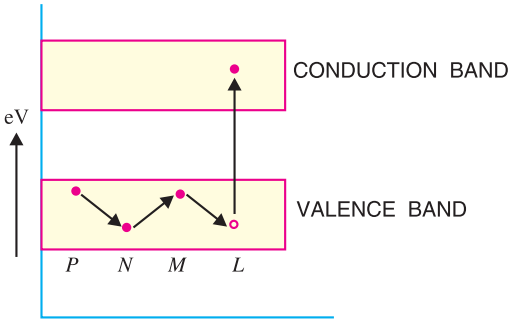


Fig. 5.9

* Note that hole acts as a virtual charge, although there is no physical charge on it.
** There is a strong tendency of semiconductor crystal to form co-valent bonds. Therefore, a hole attracts an electron from the neighbouring atom.
*** Unlike the normal current which is by free electrons.

5.8 Intrinsic Semiconductor

A semiconductor in an extremely pure form is known as an **intrinsic semiconductor**.

In an intrinsic semiconductor, even at room temperature, hole-electron pairs are created. When electric field is applied across an intrinsic semiconductor, the current conduction takes place by two processes, namely ; by *free electrons* and *holes* as shown in Fig. 5.10. The free electrons are produced due to the breaking up of some covalent bonds by thermal energy. At the same time, holes are created in the covalent bonds. Under the influence of electric field, conduction through the semiconductor is by both free electrons and holes. Therefore, the total current inside the semiconductor is the sum of currents due to free electrons and holes.

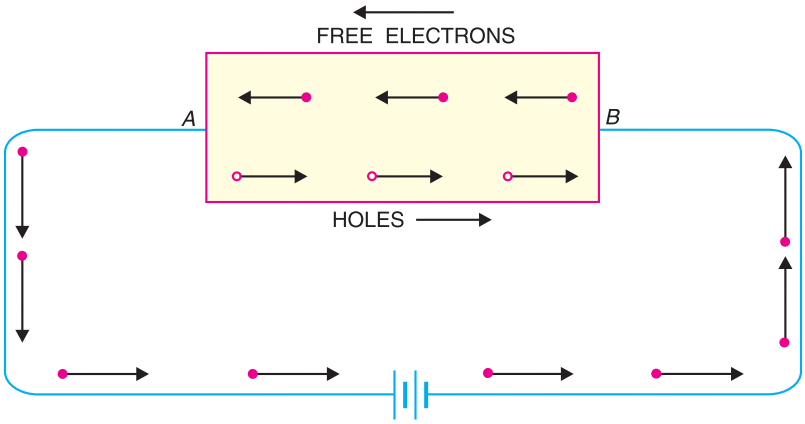


Fig. 5.10

It may be noted that current in the external wires is fully electronic *i.e.* by electrons. What about the holes ? Referring to Fig. 5.10, holes being positively charged move towards the negative terminal of supply. As the holes reach the negative terminal *B*, electrons enter the semiconductor crystal near the terminal and combine with holes, thus cancelling them. At the same time, the loosely held electrons near the positive terminal *A* are attracted away from their atoms into the positive terminal. This creates new holes near the positive terminal which again drift towards the negative terminal.

5.9 Extrinsic Semiconductor

The intrinsic semiconductor has little current conduction capability at room temperature. To be useful in electronic devices, the pure semiconductor must be altered so as to significantly increase its conducting properties. This is achieved by adding a small amount of suitable impurity to a semiconductor. It is then called *impurity* or *extrinsic semiconductor*. The process of adding impurities to a semiconductor is known as *doping*. The amount and type of such impurities have to be closely controlled during the preparation of extrinsic semiconductor. Generally, for 10^8 atoms of semiconductor, one impurity atom is added.

The purpose of adding impurity is to increase either the number of free electrons or holes in the semiconductor crystal. As we shall see, if a pentavalent impurity (having 5 valence electrons) is added to the semiconductor, a large number of free electrons are produced in the semiconductor. On the other hand, addition of trivalent impurity (having 3 valence electrons) creates a large number of holes in the semiconductor crystal. Depending upon the type of impurity added, extrinsic semiconductors are classified into:

(*i*) *n*-type semiconductor **(*ii*)** *p*-type semiconductor

5.10 *n*-type Semiconductor

When a small amount of pentavalent impurity is added to a pure semiconductor, it is known as **n-type semiconductor.**

The addition of pentavalent impurity provides a large number of free electrons in the semiconductor crystal. Typical examples of pentavalent impurities are *arsenic* (At. No. 33) and *antimony* (At. No. 51). Such impurities which produce *n*-type semiconductor are known as *donor impurities* because they donate or provide free electrons to the semiconductor crystal.

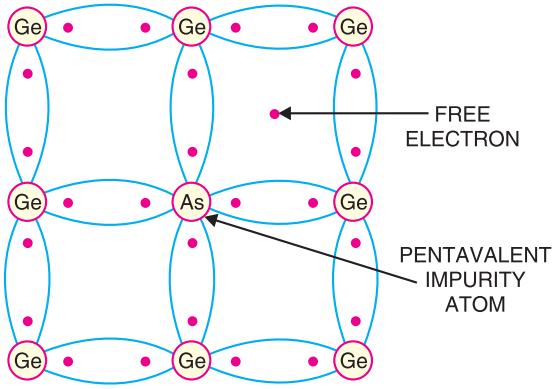


Fig. 5.11

To explain the formation of *n*-type semiconductor, consider a pure germanium crystal. We know that germanium atom has four valence electrons. When a small amount of pentavalent impurity like arsenic is added to germanium crystal, a large number of free electrons become available in the crystal. The reason is simple. Arsenic is pentavalent *i.e.* its atom has five valence electrons. An arsenic atom fits in the germanium crystal in such a way that its four valence electrons form covalent bonds with four germanium atoms. The *fifth* valence electron of arsenic atom finds no place in co-valent bonds and is thus free as shown in Fig. 5.11. Therefore, for each arsenic atom added, one free electron will be available in the germanium crystal. Though each arsenic atom provides one free electron, yet an extremely small amount of arsenic impurity provides enough atoms to supply millions of free electrons.

Fig. 5.12 shows the energy band description of *n*-type semi-conductor. The addition of pentavalent impurity has produced a number of conduction band electrons *i.e.*, free electrons. The four valence electrons of pentavalent atom form covalent bonds with four neighbouring germanium atoms. The fifth left over valence electron of the pentavalent atom cannot be accommodated in the valence band and travels to the conduction band. The following points may be noted carefully :

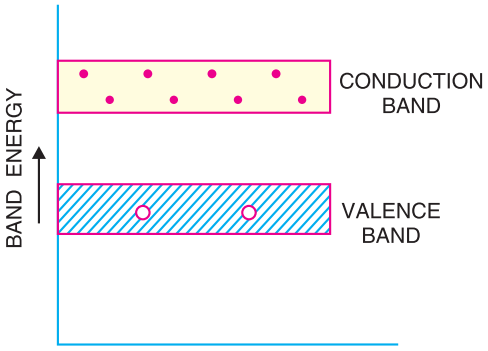


Fig. 5.12

(i) Many new free electrons are produced by the addition of pentavalent impurity.

(ii) Thermal energy of room temperature still generates a few hole-electron pairs. However, the number of free electrons provided by the pentavalent impurity far exceeds the number of holes. It is due to this predominance of electrons over holes that it is called *n*-type semiconductor (*n* stands for negative).

n-type conductivity. The current conduction in an *n*-type semiconductor is *predominantly* by free electrons *i.e.* negative charges and is called *n-type* or *electron type conductivity*. To understand *n*-type conductivity, refer to Fig. 5.13. When p.d. is applied across the *n*-type semiconductor, the free electrons (donated by impurity) in the crystal will be directed towards the positive terminal, constituting electric current. As the current flow through the crystal is by free electrons which are carriers of negative charge, therefore, this type of conductivity is called negative or *n*-type conductivity. It may be noted that conduction is just as in ordinary metals like copper.

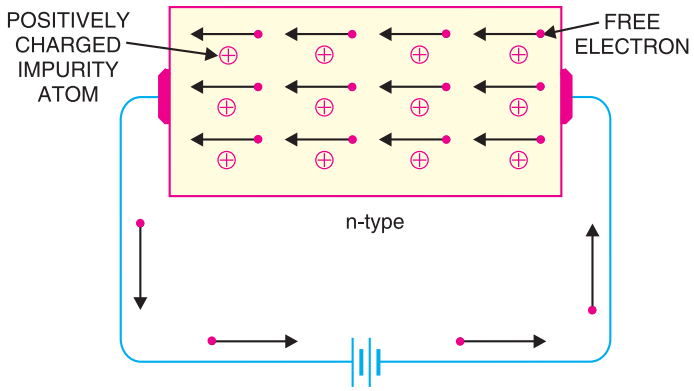


Fig. 5.13

5.11 *p*-type Semiconductor

When a small amount of trivalent impurity is added to a pure semiconductor, it is called **p-type semiconductor.**

The addition of trivalent impurity provides a large number of holes in the semiconductor. Typical examples of trivalent impurities are *gallium* (At. No. 31) and *indium* (At. No. 49). Such impurities which produce *p*-type semiconductor are known as *acceptor impurities* because the holes created can accept the electrons.

To explain the formation of *p*-type semiconductor, consider a pure germanium crystal. When a small amount of trivalent impurity like gallium is added to germanium crystal, there exists a large number of holes in the crystal. The reason is simple. Gallium is trivalent *i.e.* its atom has three valence electrons. Each atom of gallium fits into the germanium crystal but now only three co-valent bonds can be formed. It is because three valence electrons of gallium atom can form only three single co-valent bonds with three germanium atoms as shown in Fig. 5.14. In the fourth co-valent bond, only germanium atom contributes one valence electron while gallium has no valence electron to contribute as all its three valence electrons are already engaged in the co-valent bonds with neighbouring germanium atoms. In other words, fourth bond is incomplete; being short of one electron. This missing electron is called a *hole*. Therefore, for each gallium atom added, one hole is created. A small amount of gallium provides millions of holes.

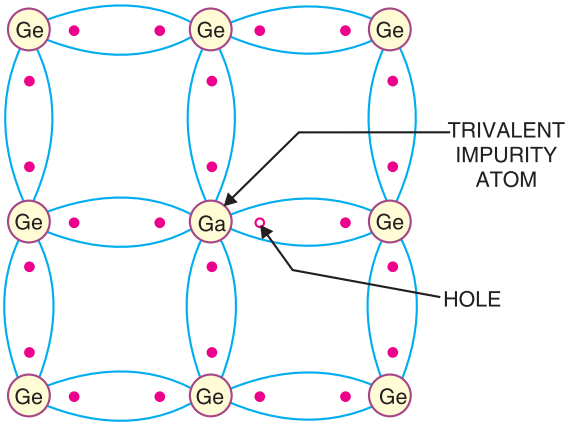


Fig. 5.14

Fig. 5.15 shows the energy band description of the *p*-type semiconductor. The addition of trivalent impurity has produced a large number of holes. However, there are a few conduction band electrons due to thermal energy associated with room temperature. But the holes far outnumber the conduction band electrons. It is due to the predominance of holes over free electrons that it is called *p*-type semiconductor (*p* stands for positive).

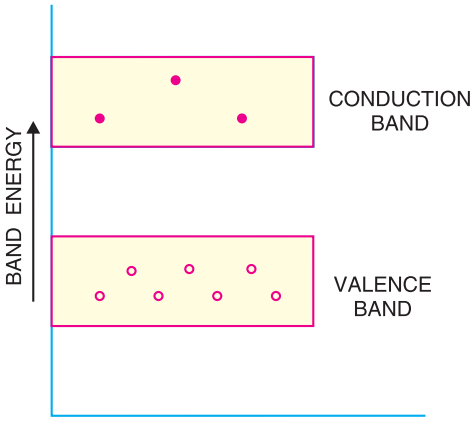


Fig. 5.15

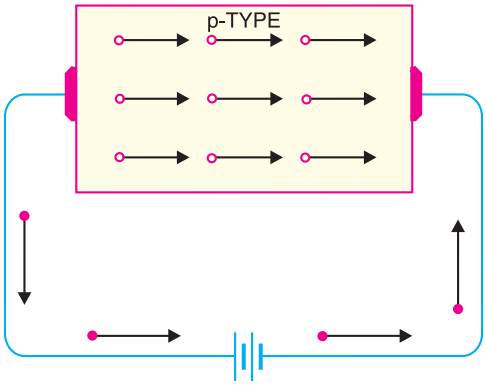


Fig. 5.16

p-type conductivity. The current conduction in *p*-type semiconductor is predominantly by holes *i.e.* positive charges and is called *p-type* or *hole-type conductivity*. To understand *p*-type conductivity, refer to Fig. 5.16. When *p.d.* is applied to the *p*-type semiconductor, the holes (donated by the impurity) are shifted from one co-valent bond to another. As the holes are positively charged, therefore, they are directed towards the negative terminal, constituting what is known as hole current. It may be noted that in *p*-type conductivity, the valence electrons move from one co-valent bond to another unlike the *n*-type where current conduction is by free electrons.

5.12 Charge on *n*-type and *p*-type Semiconductors

As discussed before, in *n*-type semiconductor, current conduction is due to excess of electrons whereas in a *p*-type semiconductor, conduction is by holes. The reader may think that *n*-type material has a net negative charge and *p*-type a net positive charge. But this conclusion is wrong. It is true that *n*-type semiconductor has excess of electrons but these extra electrons were supplied by the atoms of donor impurity and each atom of donor impurity is electrically neutral. When the impurity atom is added, the term "excess electrons" refers to an excess with regard to the number of electrons needed to fill the co-valent bonds in the semiconductor crystal. The extra electrons are free electrons and increase the conductivity of the semiconductor. The situation with regard to *p*-type semiconductor is also similar. *It follows, therefore, that n-type as well as p-type semiconductor is electrically neutral.*

5.13 Majority and Minority Carriers

It has already been discussed that due to the effect of impurity, *n*-type material has a large number of free electrons whereas *p*-type material has a large number of holes. However, it may be recalled that even at room temperature, some of the co-valent bonds break, thus releasing an equal number of free electrons and holes. An *n*-type material has its share of electron-hole pairs (released due to breaking of bonds at room temperature) but in addition has a much larger quantity of free electrons due to the effect of impurity. These impurity-caused free electrons are not associated with holes. Consequently, an *n*-type material has a large number of free electrons and a small number of holes as shown in Fig. 5.17 (*i*). The free electrons in this case are considered *majority carriers* — since the majority portion of current in *n*-type material is by the flow of free electrons — and the holes are the *minority carriers.*

Similarly, in a *p*-type material, holes outnumber the free electrons as shown in Fig. 5.17 (*ii*). Therefore, holes are the majority carriers and free electrons are the minority carriers.

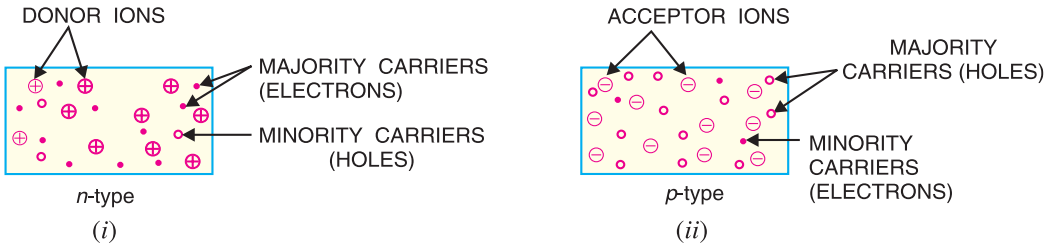


Fig. 5.17

5.14 *pn* Junction

When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called ***pn* junction.**

Most semiconductor devices contain one or more *pn* junctions. The *pn* junction is of great importance because it is in effect, the *control element* for semiconductor devices. A thorough knowledge of the formation and properties of *pn* junction can enable the reader to understand the semiconductor devices.

Formation of *pn* junction. In actual practice, the characteristic properties of *pn* junction will not be apparent if a *p*-type block is just brought in contact with *n*-type block. In fact, *pn* junction is fabricated by special techniques. One common method of making *pn* junction is called *alloying*. In this method, a small block of indium (trivalent impurity) is placed on an *n*-type germanium slab as shown in Fig. 5.18 (*i*). The system is then heated to a temperature of about 500°C. The indium and some of the germanium melt to form a small puddle of molten germanium-indium mixture as shown in Fig. 5.18 (*ii*). The temperature is then lowered and puddle begins to solidify. Under proper conditions, the atoms of indium impurity will be suitably adjusted in the germanium slab to form a single crystal. The addition of indium overcomes the excess of electrons in the *n*-type germanium to such an extent that it creates a *p*-type region.

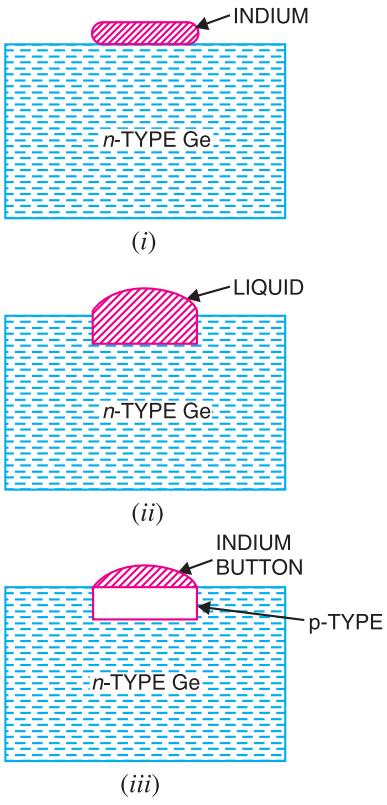
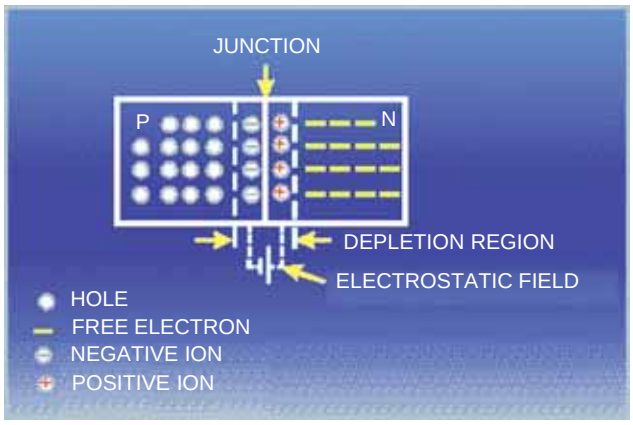


Fig. 5.18

As the process goes on, the remaining molten mixture becomes increasingly rich in indium. When all germanium has been redeposited, the remaining material appears as indium button which is frozen on to the outer surface of the crystallised portion as shown in Fig. 5.18 (*iii*). This button serves as a suitable base for soldering on leads.



5.15 Properties of *pn* Junction

At the instant of *pn*-junction formation, the free electrons near the junction in the *n* region begin to diffuse across the junction into the *p* region where they combine with holes near the junction. The result is that *n* region loses free electrons as they diffuse into the junction. This creates a layer of positive charges (pentavalent ions) near the junction. As the electrons move across the junction, the *p* region loses holes as the electrons and holes combine. The result is that there is a layer of negative charges (trivalent ions) near the junction. These two layers of positive and negative charges form the *depletion region* (or *depletion layer*). The term depletion is due to the fact that near the junction, the region is depleted (*i.e.* emptied) of *charge carries* (free electrons and holes) due to diffusion across the junction. It may be noted that depletion layer is formed very quickly and is very thin compared to the *n* region and the *p* region. For clarity, the width of the depletion layer is shown exaggerated.

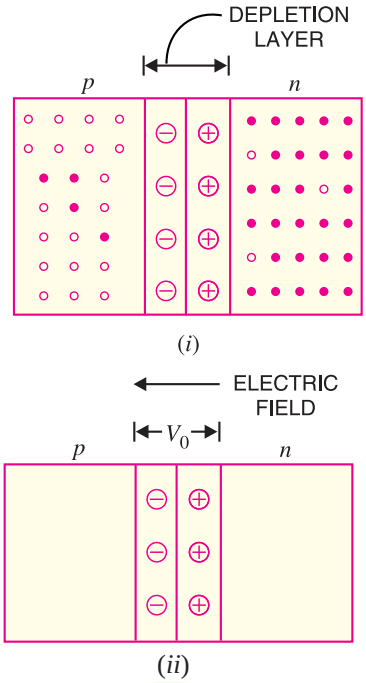


Fig. 5.19

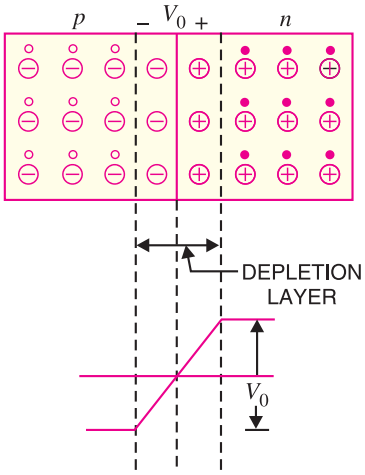


Fig. 5.20

Once *pn* junction is formed and depletion layer created, the diffusion of free electrons stops. In other words, the depletion region acts as a barrier to the further movement of free electrons across the junction. The positive and negative charges set up an electric field. This is shown by a black arrow in Fig. 5.19 (*i*). The electric field is a barrier to the free electrons in the *n*-region. There exists a potential difference across the depletion layer and is called **barrier potential** (V_0). The barrier potential of a *pn* junction depends upon several factors including the type of semiconductor material, the amount of doping and temperature. The typical barrier potential is approximately:

For silicon, $V_0 = 0.7$ V ; For germanium, $V_0 = 0.3$ V

Fig. 5.20 shows the potential (V_0) distribution curve.

5.16 Applying D.C. Voltage Across *pn* Junction or Biasing a pn Junction

In electronics, the term bias refers to the use of d.c. voltage to establish certain operating conditions

for an electronic device. In relation to a *pn* junction, there are following two bias conditions :

1. Forward biasing **2. Reverse biasing**

1. Forward biasing. *When external d.c. voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called* **forward biasing.**

To apply forward bias, connect positive terminal of the battery to *p*-type and negative terminal to *n*-type as shown in Fig. 5.21. The applied forward potential establishes an electric field which acts against the field due to potential barrier. Therefore, the resultant field is weakened and the barrier height is reduced at the junction as shown in Fig. 5.21. As potential barrier voltage is very small (0.1 to 0.3 V), therefore, a small forward voltage is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit. Therefore, current flows in the circuit. This is called *forward current.* With forward bias to *pn* junction, the following points are worth noting :

(*i*) The potential barrier is reduced and at some forward voltage (0.1 to 0.3 V), it is eliminated altogether.

(*ii*) The junction offers low resistance (called *forward resistance*, R_f) to current flow.

(*iii*) Current flows in the circuit due to the establishment of low resistance path. The magnitude of current depends upon the applied forward voltage.

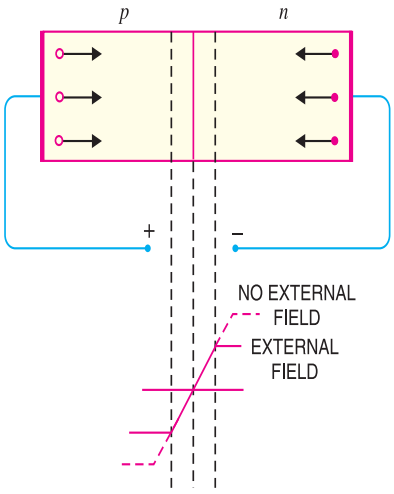


Fig. 5.21

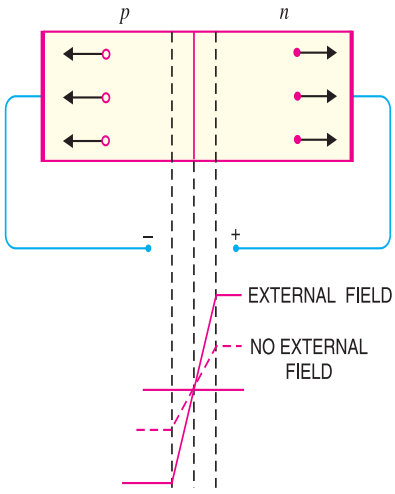


Fig. 5.22

2. Reverse biasing. *When the external d.c. voltage applied to the junction is in such a direction that potential barrier is increased, it is called* **reverse biasing.**

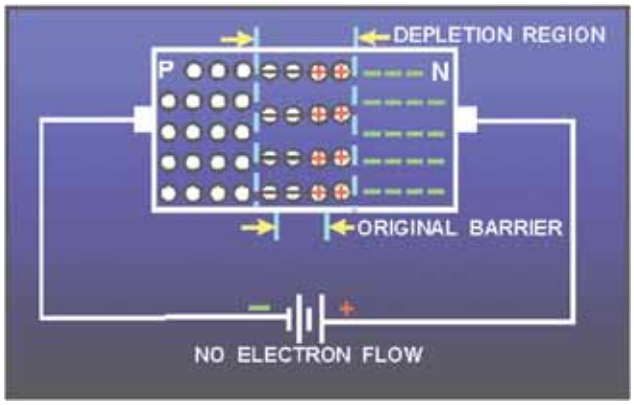
To apply reverse bias, connect negative terminal of the battery to *p*-type and positive terminal to *n*-type as shown in Fig. 5.22. It is clear that applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier. Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig. 5.22. The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence the current does not flow. With reverse bias to *pn* junction, the following points are worth noting :

(*i*) The potential barrier is increased.

(ii) The junction offers very high resistance (called *reverse resistance*, R_r) to current flow.

(iii) No current flows in the circuit due to the establishment of high resistance path.

Conclusion. From the above discussion, it follows that with reverse bias to the junction, a high resistance path is established and hence no current flow occurs. On the other hand, with forward bias to the junction, a low resistance path is set up and hence current flows in the circuit.



5.17 Current Flow in a Forward Biased pn Junction

We shall now see how current flows across *pn* junction when it is forward biased. Fig. 5.23 shows a forward biased *pn* junction. Under the influence of forward voltage, the free electrons in *n*-type move *towards the junction, leaving behind positively charged atoms. However, more electrons arrive from the negative battery terminal and enter the *n*-region to take up their places. As the free electrons reach the junction, they become **valence electrons. As valence electrons, they move through the holes in the *p*-region. The valence electrons move towards left in the *p*-region which is equivalent to the holes moving to right. When the valence electrons reach the left end of the crystal, they flow into the positive terminal of the battery.

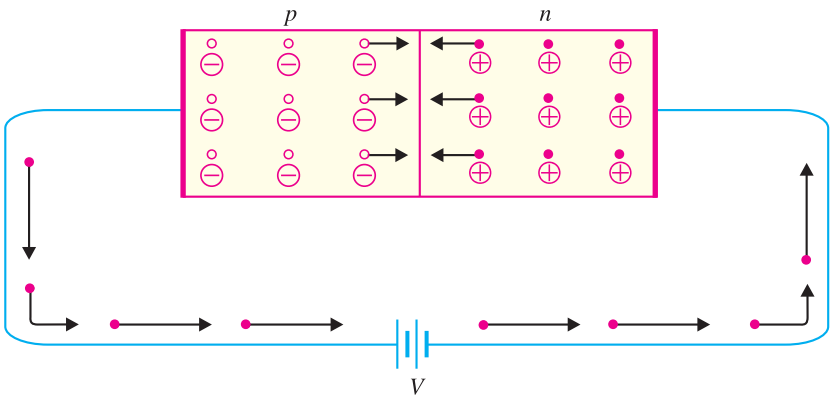


Fig. 5.23

The mechanism of current flow in a forward biased *pn* junction can be summed up as under :

(i) The free electrons from the negative terminal continue to pour into the *n*-region while the free electrons in the *n*-region move towards the junction.

(ii) The electrons travel through the *n*-region as free-electrons *i.e.* current in *n*-region is by free electrons.

* Note that negative terminal of battery is connected to *n*-type. It repels the free electrons in *n*-type towards the junction.

** A hole is in the co-valent bond. When a free electron combines with a hole, it becomes a valence electron.

(*iii*) When these electrons reach the junction, they combine with holes and become valence electrons.

(*iv*) The electrons travel through *p*-region as valence electrons *i.e.* current in the *p*-region is by holes.

(*v*) When these valence electrons reach the left end of crystal, they flow into the positive terminal of the battery.

From the above discussion, it is concluded that in *n*-type region, current is carried by free electrons whereas in *p*-type region, it is carried by holes. However, in the external connecting wires, the current is carried by free electrons.

5.18 Volt-Ampere Characteristics of *pn* Junction

Volt-ampere or *V-I* characteristic of a *pn* junction (also called a *crystal or semiconductor diode*) is the curve between voltage across the junction and the circuit current. Usually, voltage is taken along *x*-axis and current along *y*-axis. Fig. 5.24 shows the *circuit arrangement for determining the *V-I* characteristics of a *pn* junction. The characteristics can be studied under three heads, namely; *zero external voltage*, *forward bias* and *reverse bias*.

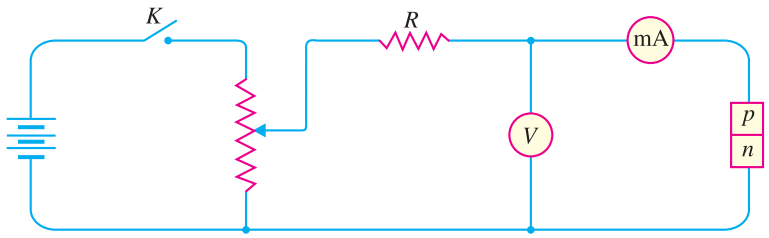


Fig. 5.24

(*i*) Zero external voltage. When the external voltage is zero, *i.e.* circuit is open at *K*, the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point *O* in Fig. 5.25.

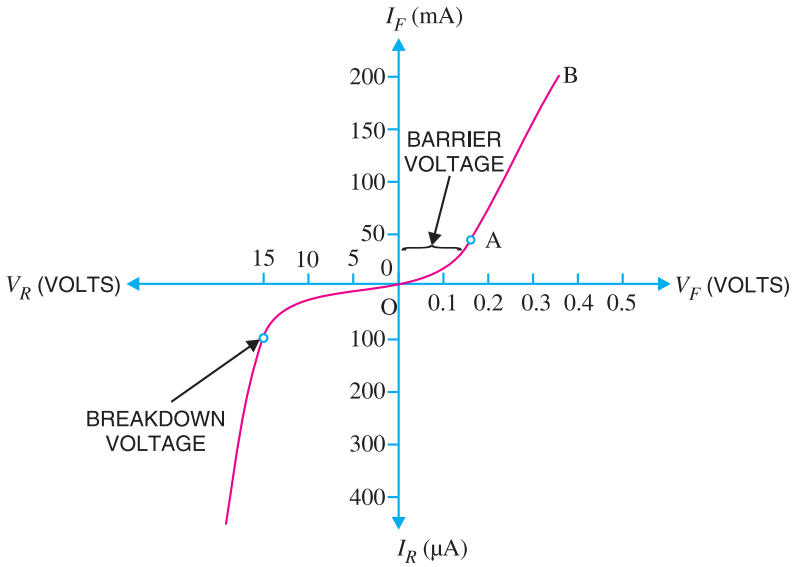


Fig. 5.25

* *R* is the current limiting resistance. It prevents the forward current from exceeding the permitted value.

(*ii*) Forward bias. With forward bias to the *pn* junction *i.e. p*-type connected to positive terminal and *n*-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7 V for Si and 0.3 V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage. Thus, a rising curve *OB* is obtained with forward bias as shown in Fig. 5.25. From the forward characteristic, it is seen that at first (*region OA*),the current increases very slowly and the curve is non-linear. It is because the external applied voltage is used up in overcoming the potential barrier. However, once the external voltage exceeds the potential barrier voltage, the *pn* junction behaves like an ordinary conductor. Therefore, the current rises very sharply with increase in external voltage (*region AB on the curve*). The curve is almost linear.

(*iii*) Reverse bias. With reverse bias to the *pn* junction *i.e. p*-type connected to negative terminal and *n*-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit. However, in practice, a very small current (of the order of μ*A*) flows in the circuit with reverse bias as shown in the reverse characteristic. This is called *reverse *saturation current* (I_s) and is due to the minority carriers. It may be recalled that there are a few free electrons in *p*-type material and a few holes in *n*-type material. These undesirable free electrons in *p*-type and holes in *n*-type are called *minority carriers*. As shown in Fig. 5.26, to these minority carriers, the applied reverse bias appears as forward bias. Therefore, a **small current flows in the reverse direction.

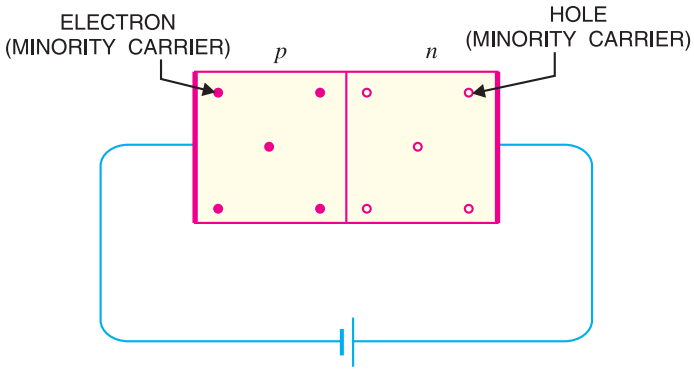


Fig. 5.26

If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms. At this stage *breakdown* of the junction occurs, characterised by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

Note. The forward current through a *pn* junction is due to the *majority carriers* produced by the impurity. However, reverse current is due to the *minority carriers* produced due to breaking of some co-valent bonds at room temperature.

5.19 Important Terms

Two important terms often used with *pn* junction (*i.e.* crystal diode) are *breakdown voltage* and *knee voltage*. We shall now explain these two terms in detail.

(*i*) Breakdown voltage. *It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.*

Under normal reverse voltage, a very little reverse current flows through a *pn* junction. However, if the reverse voltage attains a high value, the junction may break down with sudden rise in

* The term saturation comes from the fact that it reaches its maximum level quickly and does not significantly change with the increase in reverse voltage.

** Reverse current increases with reverse voltage but can generally be regarded as negligible over the working range of voltages.

reverse current. For understanding this point, refer to Fig. 5.27. Even at room temperature, some hole-electron pairs (minority carriers) are produced in the depletion layer as shown in Fig. 5.27 (*i*). With reverse bias, the electrons move towards the positive terminal of supply. At large reverse voltage, these electrons acquire high enough velocities to dislodge valence electrons from semiconductor atoms as shown in Fig. 5.27 (*ii*). The newly liberated electrons in turn free other valence electrons. In this way, we get an *avalanche* of free electrons. Therefore, the *pn* junction conducts a very large reverse current.

Once the breakdown voltage is reached, the high reverse current may damage the junction. Therefore, care should be taken that reverse voltage across a *pn* junction is always less than the breakdown voltage.

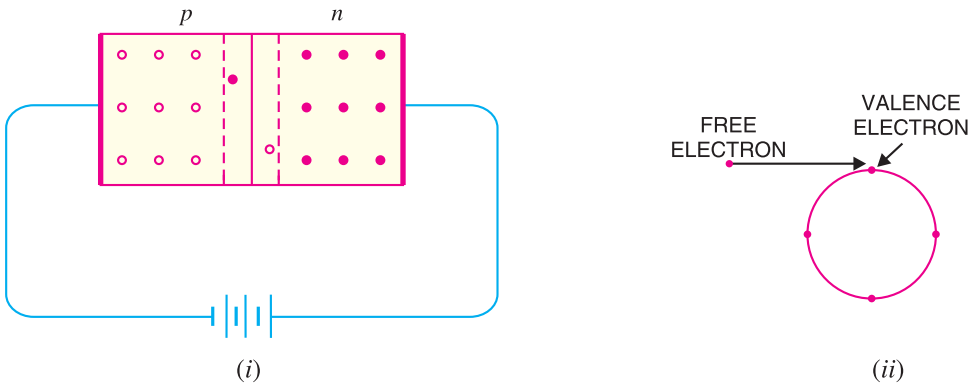


Fig. 5.27

(*ii*) Knee voltage. *It is the forward voltage at which the current through the junction starts to increase rapidly.*

When a diode is forward biased, it conducts current very slowly until we overcome the potential barrier. For silicon *pn* junction, potential barrier is 0.7 V whereas it is 0.3 V for germanium junction. It is clear from Fig. 5.28 that knee voltage for silicon diode is 0.7 V and 0.3 V for germanium diode.

Once the applied forward voltage exceeds the knee voltage, the current starts increasing rapidly. It may be added here that in order to get useful current through a *pn* junction, the applied voltage must be more than the knee voltage.

Note. The potential barrier voltage is also known as *turn-on voltage*. This is obtained by taking the straight line portion of the forward characteristic and extending it back to the horizontal axis.

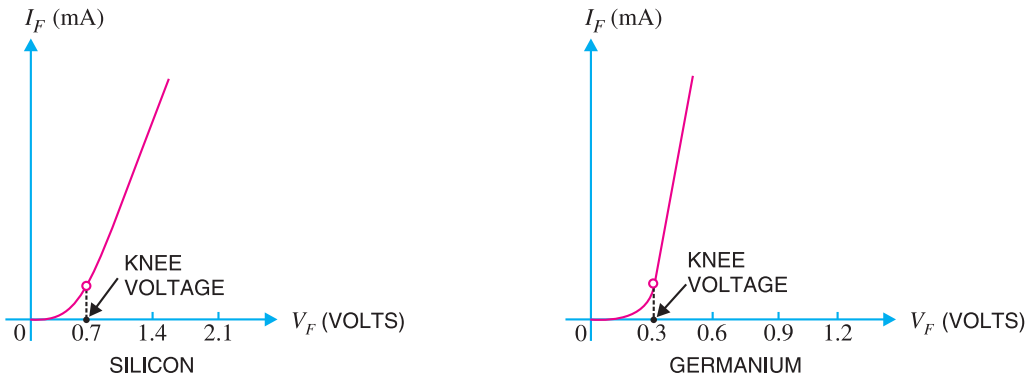


Fig. 5.28

5.20 Limitations in the Operating Conditions of *pn* Junction

Every *pn* junction has limiting values of *maximum forward current, peak inverse voltage* and *maximum power rating*. The *pn* junction will give satisfactory performance if it is operated within these limiting values. However, if these values are exceeded, the *pn* junction may be destroyed due to excessive heat.

(*i*) *Maximum forward current.* It is the highest instantaneous forward current that a *pn* junction can conduct without damage to the junction. Manufacturer's data sheet usually specifies this rating. If the forward current in a *pn* junction is more than this rating, the junction will be destroyed due to overheating.

(*ii*) *Peak inverse voltage (PIV).* It is the maximum reverse voltage that can be applied to the *pn* junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service. A *pn* junction *i.e.* a crystal diode is used as a rectifier to change alternating current into direct current. In such applications, care should be taken that reverse voltage across the diode during negative half-cycle of a.c. does not exceed the PIV of diode.

(*iii*) *Maximum power rating.* It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction. This is a very important consideration and is invariably specified by the manufacturer in the data sheet.

MULTIPLE-CHOICE QUESTIONS

1. A semiconductor is formed by ..... bonds.
(*i*) covalent (*ii*) electrovalent
(*iii*) co-ordinate (*iv*) none of the above

2. A semiconductor has ..... temperature coefficient of resistance.
(*i*) positive (*ii*) zero
(*iii*) negative (*iv*) none of the above

3. The most commonly used semiconductor is .....
(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) sulphur

4. A semiconductor has generally ..... valence electrons.
(*i*) 2 (*ii*) 3
(*iii*) 6 (*iv*) 4

5. The resistivity of pure germanium under standard conditions is about .....
(*i*) 6×10^4 Ω cm (*ii*) 60 Ω cm
(*iii*) 3×10^6 Ω cm (*iv*) 6×10^{-4} Ω cm

6. The resistivity of pure silicon is about .....
(*i*) 100 Ω cm (*ii*) 6000 Ω cm
(*iii*) 3×10^5 Ω cm (*iv*) 1.6×10^{-8} Ω cm

7. When a pure semiconductor is heated, its resistance .....
(*i*) goes up (*ii*) goes down
(*iii*) remains the same (*iv*) cannot say

8. The strength of a semiconductor crystal comes from .....
(*i*) forces between nuclei
(*ii*) forces between protons
(*iii*) electron-pair bonds
(*iv*) none of the above

9. When a pentavalent impurity is added to a pure semiconductor, it becomes .....
(*i*) an insulator
(*ii*) an intrinsic semiconductor
(*iii*) *p*-type semiconductor
(*iv*) *n*-type semiconductor

10. Addition of pentavalent impurity to a semiconductor creates many .....
(*i*) free electrons (*ii*) holes
(*iii*) valence electrons
(*iv*) bound electrons

11. A pentavalent impurity has ..... valence electrons.
(*i*) 3 (*ii*) 5
(*iii*) 4 (*iv*) 6

12. An *n*-type semiconductor is .....
(*i*) positively charged
(*ii*) negatively charged

(*iii*) electrically neutral
(*iv*) none of the above

13. A trivalent impurity has ..... valence electrons.
(*i*) 4 (*ii*) 5
(*iii*) 6 (*iv*) 3

14. Addition of trivalent impurity to a semiconductor creates many .....
(*i*) holes (*ii*) free electrons
(*iii*) valence electrons
(*iv*) bound electrons

15. A hole in a semiconductor is defined as .....
(*i*) a free electron
(*ii*) the incomplete part of an electron pair bond
(*iii*) a free proton
(*iv*) a free neutron

16. The impurity level in an extrinsic semiconductor is about ..... of pure semiconductor.
(*i*) 10 atoms for 10^8 atoms
(*ii*) 1 atom for 10^8 atoms
(*iii*) 1 atom for 10^4 atoms
(*iv*) 1 atom for 100 atoms

17. As the doping to a pure semiconductor increases, the bulk resistance of the semiconductor .....
(*i*) remains the same
(*ii*) increases
(*iii*) decreases
(*iv*) none of the above

18. A hole and electron in close proximity would tend to .....
(*i*) repel each other
(*ii*) attract each other
(*iii*) have no effect on each other
(*iv*) none of the above

19. In a semiconductor, current conduction is due .....
(*i*) only to holes
(*ii*) only to free electrons
(*iii*) to holes and free electrons
(*iv*) none of the above

20. The random motion of holes and free electrons due to thermal agitation is called .....
(*i*) diffusion (*ii*) pressure
(*iii*) ionisation (*iv*) none of the above

21. A forward biased *pn* junction has a resistance of the .....
(*i*) order of Ω (*ii*) order of kΩ
(*iii*) order of MΩ (*iv*) none of the above

22. The battery connections required to forward bias a *pn* junction are .....
(*i*) +ve terminal to *p* and –ve terminal to *n*
(*ii*) –ve terminal to *p* and +ve terminal to *n*
(*iii*) –ve terminal to *p* and –ve terminal to *n*
(*iv*) none of the above

23. The barrier voltage at a *pn* junction for germanium is about .....
(*i*) 3.5 V (*ii*) 3V
(*iii*) zero (*iv*) 0.3 V

24. In the depletion region of a *pn* junction, there is a shortage of .....
(*i*) acceptor ions (*ii*) holes and electrons
(*iii*) donor ions (*iv*) none of the above

25. A reverse biased *pn* junction has .....
(*i*) very narrow depletion layer
(*ii*) almost no current
(*iii*) very low resistance
(*iv*) large current flow

26. A *pn* junction acts as a .....
(*i*) controlled switch
(*ii*) bidirectional switch
(*iii*) unidirectional switch
(*iv*) none of the above

27. A reverse biased *pn* junction has resistance of the.....
(*i*) order of Ω (*ii*) order of kΩ
(*iii*) order of MΩ (*iv*) none of the above

28. The leakage current across a *pn* junction is due to .....
(*i*) minority carriers
(*ii*) majority carriers
(*iii*) junction capacitance
(*iv*) none of the above

29. When the temperature of an extrinsic semiconductor is increased, the pronounced effect is on .....
(*i*) junction capacitance

(*ii*) minority carriers
(*iii*) majority carriers
(*iv*) none of the above

30. With forward bias to a *pn* junction, the width of depletion layer .....
(*i*) decreases (*ii*) increases
(*iii*) remains the same
(*iv*) none of the above

31. The leakage current in a *pn* junction is of the order of .....
(*i*) A (*ii*) mA
(*iii*) kA (*iv*) μA

32. In an intrinsic semiconductor, the number of free electrons .....
(*i*) equals the number of holes
(*ii*) is greater than the number of holes
(*iii*) is less than the number of holes
(*iv*) none of the above

33. At room temperature, an intrinsic semiconductor has .....
(*i*) many holes only
(*ii*) a few free electrons and holes
(*iii*) many free electrons only
(*iv*) no holes or free electrons

34. At absolute temperature, an intrinsic semiconductor has .....
(*i*) a few free electrons
(*ii*) many holes
(*iii*) many free electrons
(*iv*) no holes or free electrons

35. At room temperature, an intrinsic silicon crystal acts approximately as .....
(*i*) a battery
(*ii*) a conductor
(*iii*) an insulator
(*iv*) a piece of copper wire

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*iii*)	**3.** (*ii*)	**4.** (*iv*)	**5.** (*ii*)
6. (*ii*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*iv*)	**10.** (*i*)
11. (*ii*)	**12.** (*iii*)	**13.** (*iv*)	**14.** (*i*)	**15.** (*ii*)
16. (*ii*)	**17.** (*iii*)	**18.** (*ii*)	**19.** (*iii*)	**20.** (*i*)
21. (*i*)	**22.** (*i*)	**23.** (*iv*)	**24.** (*ii*)	**25.** (*ii*)
26. (*iii*)	**27.** (*iii*)	**28.** (*i*)	**29.** (*ii*)	**30.** (*i*)
31. (*iv*)	**32.** (*i*)	**33.** (*ii*)	**34.** (*iv*)	**35.** (*iii*)

Chapter Review Topics

1. What do you understand by a semi-conductor ? Discuss some important properties of semiconductors.
2. Which are the most commonly used semiconductors and why ?
3. Give the energy band description of semiconductors.
4. Discuss the effect of temperature on semiconductors.
5. Give the mechanism of hole current flow in a semiconductor.
6. What do you understand by intrinsic and extrinsic semiconductors ?
7. What is a *pn* junction ? Explain the formation of potential barrier in a *pn* junction.
8. Discuss the behaviour of a *pn* junction under forward and reverse biasing.
9. Draw and explain the *V-I* characteristics of a *pn* junction.
10. Write short notes on the following :
(*i*) Breakdown voltage
(*ii*) Knee voltage
(*iii*) Limitations in the operating conditions of *pn* junction

Discussion Questions

1. Why is a semiconductor an insulator at ordinary temperature ?
2. Why are electron carriers present in *p*-type semiconductor ?
3. Why is silicon preferred to germanium in the manufacture of semiconductor devices ?
4. What is the importance of peak inverse voltage ?

Top

Contents

6

Semiconductor Diode

INTRODUCTION

It has already been discussed in the previous chapter that a *pn* junction conducts current easily when forward biased and practically no current flows when it is reverse biased. This unilateral conduction characteristic of *pn* junction (*i.e.* semiconductor diode) is similar to that of a vacuum diode. Therefore, like a vacuum diode, a semiconductor diode can also accomplish the job of *rectification* *i.e.* change alternating current to direct current. However, semiconductor diodes have become more *popular as they are smaller in size, cheaper and robust and usually operate with greater efficiency. In this chapter, we shall focus our attention on the circuit performance and applications of semiconductor diodes.

* On the other hand, vacuum diodes can withstand high reverse voltages and can operate at fairly high temperatures.

6.1 Semiconductor Diode

A pn junction is known as a **semi-conductor** *or* ***crystal diode**.

The outstanding property of a crystal diode to conduct current in one direction only permits it to be used as a rectifier. A crystal diode is usually represented by the schematic symbol shown in Fig. 6.1. The arrow in the symbol indicates the direction of easier conventional current flow.

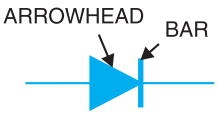


Fig. 6.1

A crystal diode has two terminals. When it is connected in a circuit, one thing to decide is whether the diode is forward or reverse biased. There is an easy rule to ascertain it. If the external circuit is trying to push the conventional current in the direction of arrow, the diode is forward biased. On the other hand, if the conventional current is trying to flow opposite to arrowhead, the diode is reverse biased. Putting in simple words :

(*i*) If *arrowhead* of diode symbol is *positive w.r.t. bar* of the symbol, the diode is forward biased.

(*ii*) If the *arrowhead* of diode symbol is *negative w.r.t. bar*, the diode is reverse biased.

Identification of crystal diode terminals. While using a crystal diode, it is often necessary to know which end is arrowhead and which end is bar. For this purpose, the following methods are available :

(*i*) Some manufacturers actually paint the symbol on the body of the diode *e.g. BY*127, *BY*114 crystal diodes manufactured by *BEL* [See Fig. 6.2 (*i*)].

Fig. 6.2

(*ii*) Sometimes, red and blue marks are used on the body of the crystal diode. Red mark denotes arrow whereas blue mark indicates bar *e.g. OA80* crystal diode [See Fig. 6.2 (*ii*)].

6.2 Crystal Diode as a Rectifier

Fig. 6.3 illustrates the rectifying action of a crystal diode. The a.c. input voltage to be rectified, the diode and load R_L are connected in series. The d.c. output is obtained across the load as explained in the following discussion. During the positive half-cycle of a.c. input voltage, the arrowhead becomes positive *w.r.t.* bar. Therefore, diode is forward biased and conducts current in the circuit. The result is that positive half-cycle of input voltage appears across R_L as shown. However, during the negative half-cycle of input a.c. voltage, the diode becomes reverse biased because now the arrowhead is negative *w.r.t.* bar. Therefore, diode does not conduct and no voltage appears across load R_L. The result is that output consists of positive half-cycles of input a.c. voltage while the negative half-cycles are suppressed. In this way, crystal diode has been able to do rectification i.e. change a.c. into d.c. It may be seen that output across R_L is pulsating d.c.

* So called because *pn* junction is grown out of a crystal.

It is interesting to see that behaviour of diode is like a *switch*. When the diode is forward biased, it behaves like a closed switch and connects the a.c. supply to the load R_L. However, when the diode is reverse biased, it behaves like an open switch and disconnects the a.c. supply from the load R_L. This switching action of diode permits only the positive half-cycles of input a.c. voltage to appear across R_L.

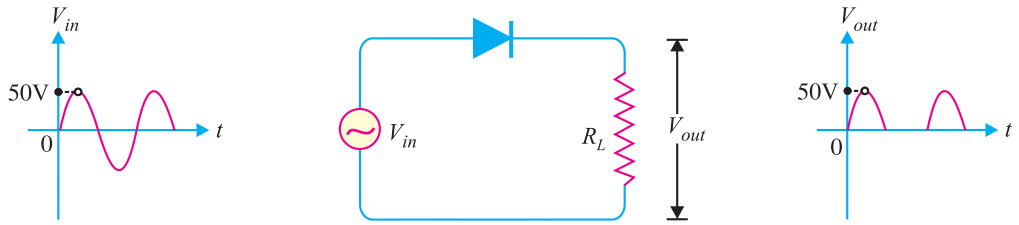


Fig. 6.3

Example 6.1. *In each diode circuit of Fig. 6.4, find whether the diodes are forward or reverse biased.*

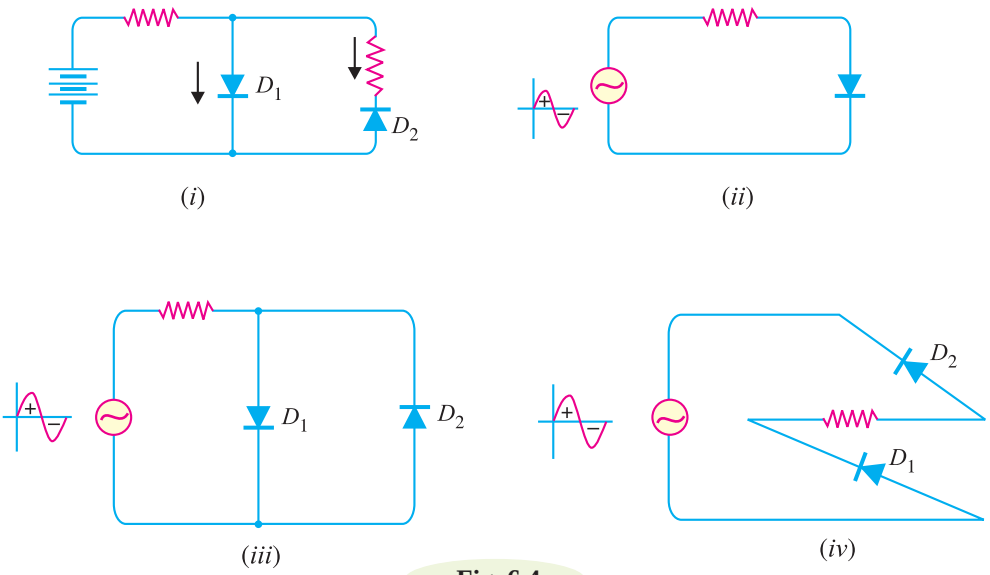


Fig. 6.4

Solution.

(*i*) Refer to Fig. 6.4 (*i*). The conventional current coming out of battery flows in the branch circuits. In diode D_1, the conventional current flows in the direction of arrowhead and hence this diode is forward biased. However, in diode D_2,the conventional current flows opposite to arrowhead and hence this diode is reverse biased.

(*ii*) Refer to Fig. 6.4 (*ii*). During the positive half-cycle of input a.c. voltage, the conventional current flows in the direction of arrowhead and hence diode is forward biased. However, during the negative half-cycle of input a.c. voltage, the diode is reverse biased.

(*iii*) Refer to Fig. 6.4 (*iii*). During the positive half-cycle of input a.c. voltage, conventional current flows in the direction of arrowhead in D_1 but it flows opposite to arrowhead in D_2. Therefore, during positive half-cycle, diode D_1 is forward biased and diode D_2 reverse biased. However, during the negative half-cycle of input a.c. voltage, diode D_2 is forward biased and D_1 is reverse biased.

(*iv*) Refer to Fig. 6.4 (*iv*). During the positive half-cycle of input a.c. voltage, both the diodes are reverse biased. However, during the negative half-cycle of input a.c. voltage, both the diodes are forward biased.

6.3 Resistance of Crystal Diode

It has already been discussed that a forward biased diode conducts easily whereas a reverse biased diode practically conducts no current. It means that *forward resistance* of a diode is quite small as compared with its *reverse resistance.*

1. Forward resistance. The resistance offered by the diode to forward bias is known as *forward resistance*. This resistance is not the same for the flow of direct current as for the changing current. Accordingly; this resistance is of two types, namely; *d.c. forward resistance* and *a.c. forward resistance.*

(*i*) *d.c. forward resistance.* It is the opposition offered by the diode to the direct current. It is measured by the ratio of d.c. voltage across the diode to the resulting d.c. current through it. Thus, referring to the forward characteristic in Fig. 6.5, it is clear that when forward voltage is *OA*, the forward current is *OB*.

$$\therefore \quad \text{d.c. forward resistance, } R_f = \frac{OA}{OB}$$

(*ii*) *a.c. forward resistance.* It is the opposition offered by the diode to the changing forward current. It is measured by the ratio of change in voltage across diode to the resulting change in current through it *i.e.*

$$\text{a.c. forward resistance, } r_f = \frac{\text{Change in voltage across diode}}{\text{Corresponding change in current through diode}}$$

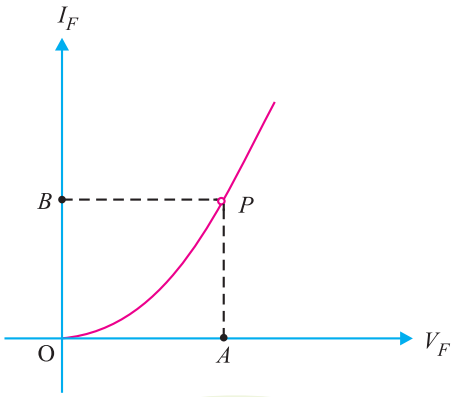


Fig. 6.5

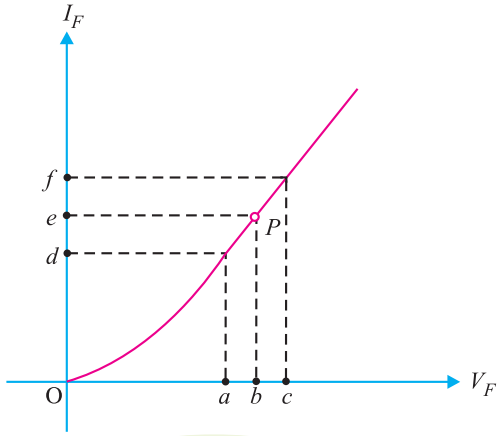


Fig. 6.6

The a.c. forward resistance is more significant as the diodes are generally used with alternating voltages. The a.c. forward resistance can be determined from the forward characteristic as shown in Fig. 6.6. If *P* is the operating point at any instant, then forward voltage is *ob* and forward current is *oe*. To find the a.c. forward resistance, vary the forward voltage on both sides of the operating point equally as shown in Fig. 6.6 where $ab = bc$. It is clear from this figure that :

For forward voltage *oa*, circuit current is *od*.

For forward voltage *oc*, circuit current is *of*.

$$\therefore \quad \text{a.c. forward resistance, } r_f = \frac{\text{Change in forward voltage}}{\text{Change in forward current}} = \frac{oc - oa}{of - od} = \frac{ac}{df}$$

It may be mentioned here that forward resistance of a crystal diode is very small, ranging from 1 to 25 Ω.

2. Reverse resistance. The resistance offered by the diode to the reverse bias is known as *reverse resistance*. It can be d.c. reverse resistance or a.c. reverse resistance depending upon whether the reverse bias is direct or changing voltage. Ideally, the reverse resistance of a diode is infinite. However, in practice, the reverse resistance is not infinite because for any value of reverse bias, there does exist a small leakage current. It may be emphasised here that reverse resistance is very large compared to the forward resistance. In germanium diodes, the ratio of reverse to forward resistance is 40000 : 1 while for silicon this ratio is 1000000 : 1.

6.4 Equivalent Circuit of Crystal Diode

It is generally profitable to replace a device or system by its equivalent circuit. An equivalent circuit of a device (*e.g.* crystal diode, transistor etc.) is a combination of electric elements, which when connected in a circuit, acts exactly as does the device when connected in the same circuit. Once the device is replaced by its equivalent circuit, the resulting network can be solved by traditional circuit analysis techniques. We shall now find the equivalent circuit of a crystal diode.

(*i*) *Approximate Equivalent circuit. When the forward voltage V_F is applied across a diode, it will not conduct till the potential barrier V_0 at the junction is overcome. When the forward voltage exceeds the potential barrier voltage, the diode starts conducting as shown in Fig. 6.7 (*i*). The forward current I_f flowing through the diode causes a voltage drop in its internal resistance r_f. Therefore, the forward voltage V_F applied across the *actual* diode has to overcome :

(*a*) potential barrier V_0

(*b*) internal drop $I_f r_f$

$$\therefore \qquad V_F = V_0 + I_f r_f$$

For a silicon diode, $V_0 = 0.7$ V whereas for a germanium diode, $V_0 = 0.3$ V.

Therefore, approximate equivalent circuit for a crystal diode is a switch in series with a battery V_0 and internal resistance r_f as shown in Fig. 6.7 (*ii*). This approximate equivalent circuit of a diode is very helpful in studying the performance of the diode in a circuit.

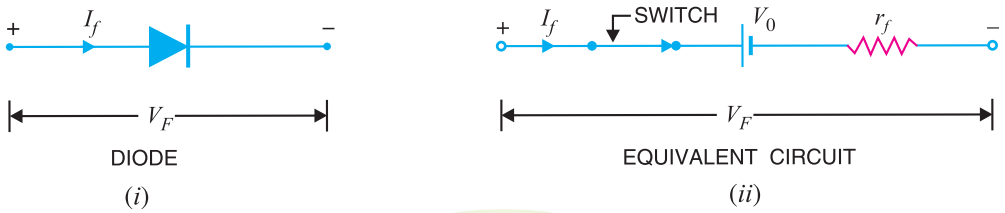


Fig. 6.7

(*ii*) Simplified Equivalent circuit. For most applications, the internal resistance r_f of the crystal diode can be ignored in comparison to other elements in the equivalent circuit. The equivalent circuit then reduces to the one shown in Fig. 6.8 (*ii*). This simplified equivalent circuit of the crystal diode is frequently used in diode-circuit analysis.

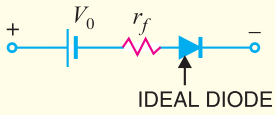
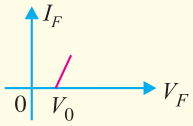
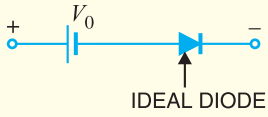
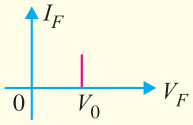
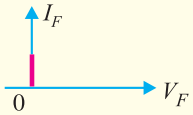
Fig. 6.8

* We assume here that *V*/*I* characteristic of crystal diode is linear.

(*iii*) Ideal diode model. An ideal diode is one which behaves as a perfect conductor when forward biased and as a perfect insulator when reverse biased. Obviously, in such a hypothetical situation, forward resistance $r_f = 0$ and potential barrier V_0 is considered negligible. It may be mentioned here that although ideal diode is never found in practice, yet diode circuit analysis is made on this basis. *Therefore, while discussing diode circuits, the diode will be assumed ideal unless and until stated otherwise.*

6.5 Crystal Diode Equivalent Circuits

It is desirable to sum up the various models of crystal diode equivalent circuit in the tabular form given below:

S.No.	Type	Model	Characteristic
1.	Approximate model		
2.	Simplified model		
3.	Ideal Model		

Example 6.2. *An a.c. voltage of peak value 20 V is connected in series with a silicon diode and load resistance of 500 Ω. If the forward resistance of diode is 10 Ω, find :*

(i) peak current through diode *(ii) peak output voltage*

What will be these values if the diode is assumed to be ideal ?

Solution.

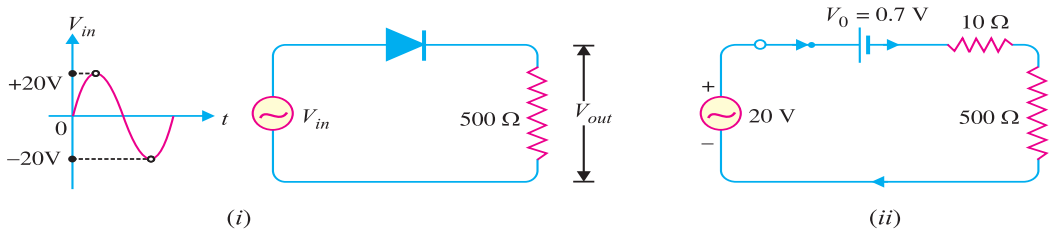
Peak input voltage = 20 V

Forward resistance, r_f = 10 Ω

Load resistance, R_L = 500 Ω

Potential barrier voltage, V_0 = 0.7 V

The diode will conduct during the positive half-cycles of a.c. input voltage only. The equivalent circuit is shown in Fig. 6.9 (*ii*).



(*i*) (*ii*)

Fig. 6.9

(*i*) The peak current through the diode will occur at the instant when the input voltage reaches positive peak *i.e.* $V_{in} = V_F = 20$ V.

$$\therefore \quad V_F = V_0 + (I_f)_{peak}\,[r_f + R_L] \qquad ...(i)$$

$$\text{or} \quad (I_f)_{peak} = \frac{V_F - V_0}{r_f + R_L} = \frac{20 - 0.7}{10 + 500} = \frac{19.3}{510}\text{ A} = \mathbf{37.8\ mA}$$

(*ii*) Peak output voltage $= (I_f)_{peak} \times R_L = 37.8\text{ mA} \times 500\ \Omega = \mathbf{18.9\ V}$

Ideal diode. For an ideal diode, put $V_0 = 0$ and $r_f = 0$ in equation (*i*).

$$\therefore \quad V_F = (I_f)_{peak} \times R_L$$

$$\text{or} \quad (I_f)_{peak} = \frac{V_F}{R_L} = \frac{20\text{ V}}{500\ \Omega} = \mathbf{40\ mA}$$

Peak output voltage $= (I_f)_{peak} \times R_L = 40\text{ mA} \times 500\ \Omega = \mathbf{20\ V}$

Comments. It is clear from the above example that output voltage is *nearly* the same whether the actual diode is used or the diode is considered ideal. This is due to the fact that input voltage is quite large as compared with V_0 and voltage drop in r_f. Therefore, nearly the whole input forward voltage appears across the load. For this reason, diode circuit analysis is generally made on the ideal diode basis.

Example 6.3. *Find the current through the diode in the circuit shown in Fig. 6.10 (i). Assume the diode to be ideal.*

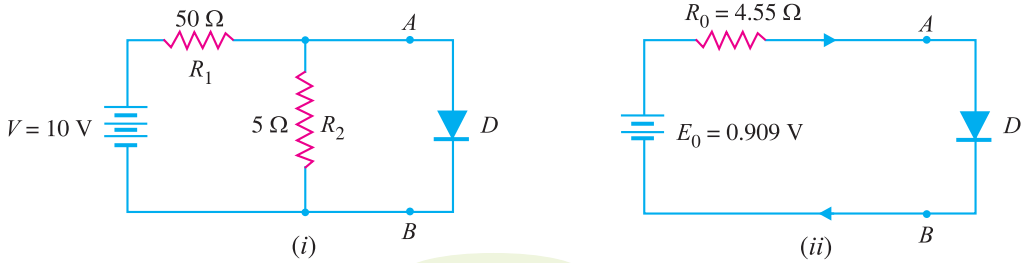


Fig. 6.10

Solution. We shall use Thevenin's theorem to find current in the diode. Referring to Fig. 6.10(*i*),

E_0 = Thevenin's voltage

= Open circuited voltage across AB with diode removed

$$= \frac{R_2}{R_1 + R_2} \times V = \frac{5}{50 + 5} \times 10 = 0.909\text{ V}$$

R_0 = Thevenin's resistance

= Resistance at terminals AB with diode removed and battery replaced by a short circuit

$$= \frac{R_1\,R_2}{R_1 + R_2} = \frac{50 \times 5}{50 + 5} = 4.55\ \Omega$$

Fig. 6.10 (*ii*) shows Thevenin's equivalent circuit. Since the diode is ideal, it has zero resistance.

$$\therefore \quad \text{Current through diode} = \frac{E_0}{R_0} = \frac{0.909}{4.55} = 0.2\text{ A} = \mathbf{200\ mA}$$

Example 6.4. *Calculate the current through 48 Ω resistor in the circuit shown in Fig. 6.11 (i). Assume the diodes to be of silicon and forward resistance of each diode is 1 Ω.*

Solution. Diodes D_1 and D_3 are forward biased while diodes D_2 and D_4 are reverse biased. We can, therefore, consider the branches containing diodes D_2 and D_4 as "open". Replacing diodes D_1 and D_3 by their equivalent circuits and making the branches containing diodes D_2 and D_4 open, we get the circuit shown in Fig. 6.11 (*ii*). Note that for a silicon diode, the barrier voltage is 0.7 V.

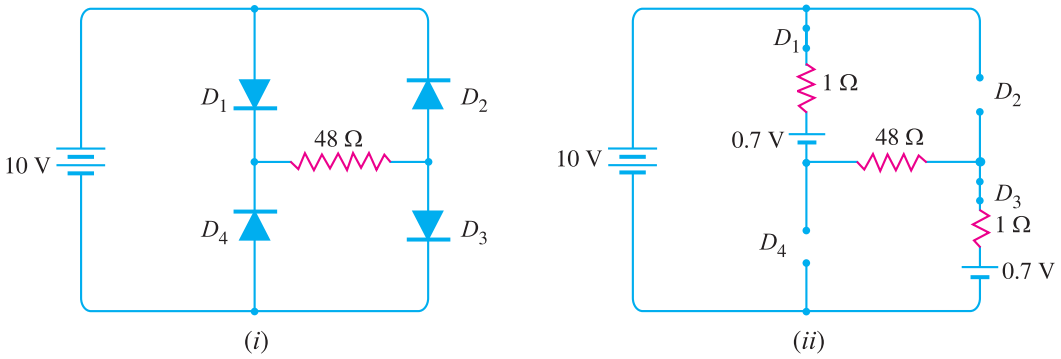


Fig. 6.11

Net circuit voltage $= 10 - 0.7 - 0.7 = 8.6$ V

Total circuit resistance $= 1 + 48 + 1 = 50\ \Omega$

$\therefore$ Circuit current $= 8.6/50 = 0.172$ A $=$ **172 mA**

Example 6.5. *Determine the current I in the circuit shown in Fig. 6.12 (i). Assume the diodes to be of silicon and forward resistance of diodes to be zero.*

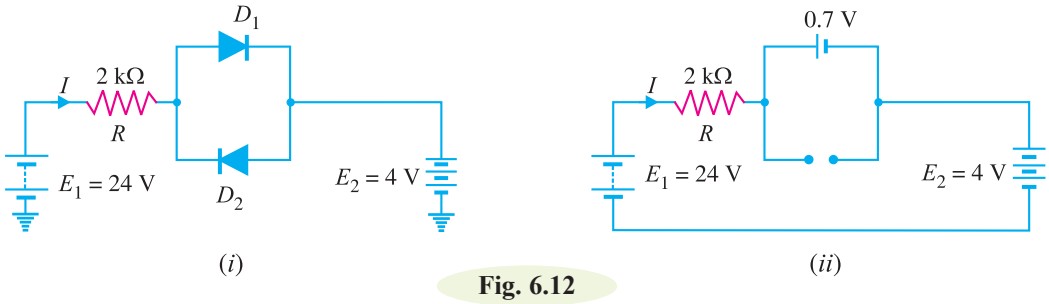


Fig. 6.12

Solution. The conditions of the problem suggest that diode D_1 is forward biased and diode D_2 is reverse biased. We can, therefore, consider the branch containing diode D_2 as open as shown in Fig. 6.12 (*ii*). Further, diode D_1 can be replaced by its simplified equivalent circuit.

$$\therefore \quad I = \frac{E_1 - E_2 - V_0}{R} = \frac{24 - 4 - 0.7}{2\ \text{k}\Omega} = \frac{19.3\ \text{V}}{2\ \text{k}\Omega} = \textbf{9.65 mA}$$

Example 6.6. *Find the voltage V_A in the circuit shown in Fig. 6.13 (i). Use simplified model.*

Fig. 6.13

Solution. It appears that when the applied voltage is switched on, both the diodes will turn "on". But that is not so. When voltage is applied, germanium diode ($V_0 = 0.3$ V) will turn on first and a level of 0.3 V is maintained across the parallel circuit. The silicon diode never gets the opportunity to have 0.7 V across it and, therefore, remains in open-circuit state as shown in Fig. 6.13 (*ii*).

$$\therefore \qquad V_A = 20 - 0.3 = \mathbf{19.7\ V}$$

Example 6.7. *Find V_Q and I_D in the network shown in Fig. 6.14 (i). Use simplified model.*

Solution. Replace the diodes by their simplified models. The resulting circuit will be as shown in Fig. 6.14 (*ii*). By symmetry, current in each branch is I_D so that current in branch CD is $2I_D$. Applying Kirchhoff's voltage law to the closed circuit $ABCDA$, we have,

$$-0.7 - I_D \times 2 - 2I_D \times 2 + 10 = 0 \qquad (I_D \text{ in mA})$$

or $$6I_D = 9.3$$

$$\therefore \qquad I_D = \frac{9.3}{6} = \mathbf{1.55\ mA}$$

Also $$V_Q = (2I_D) \times 2\ \text{k}\Omega = (2 \times 1.55\ \text{mA}) \times 2\ \text{k}\Omega = \mathbf{6.2\ V}$$

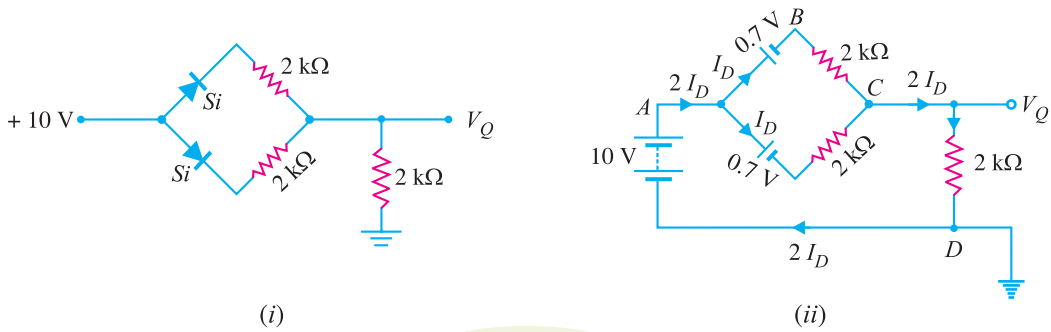


Fig. 6.14

Example 6.8. *Determine current through each diode in the circuit shown in Fig. 6.15 (i). Use simplified model. Assume diodes to be similar.*

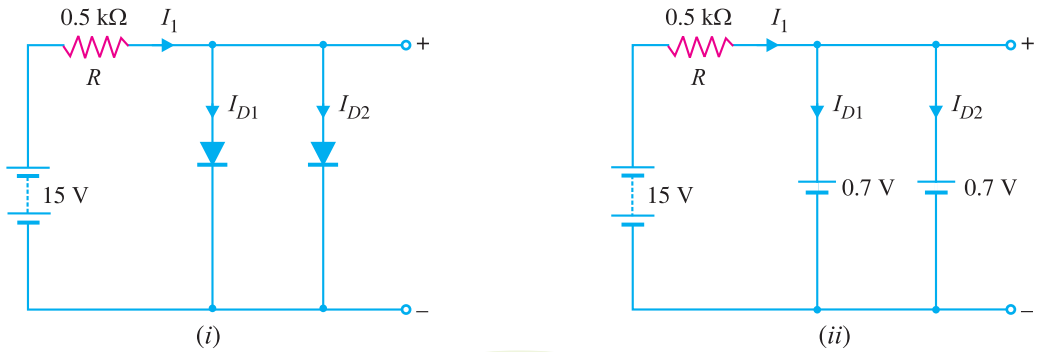


Fig. 6.15

Solution. The applied voltage forward biases each diode so that they conduct current in the same direction. Fig. 6.15 (*ii*) shows the equivalent circuit using simplified model. Referring to Fig. 6.15 (*ii*),

$$I_1 = \frac{\text{Voltage across } R}{R} = \frac{15 - 0.7}{0.5\ \text{k}\Omega} = 28.6\ \text{mA}$$

Since the diodes are similar, $I_{D1} = I_{D2} = \frac{I_1}{2} = \frac{28.6}{2} = \mathbf{14.3\ mA}$

Comments. Note the use of placing the diodes in parallel. If the current rating of each diode is 20

20 mA and a single diode is used in this circuit, a current of 28.6 mA would flow through the diode, thus damaging the device. By placing them in parallel, the current is limited to a safe value of 14.3 mA for the same terminal voltage.

Example 6.9. *Determine the currents I_1, I_2 and I_3 for the network shown in Fig. 6.16(i). Use simplified model for the diodes.*

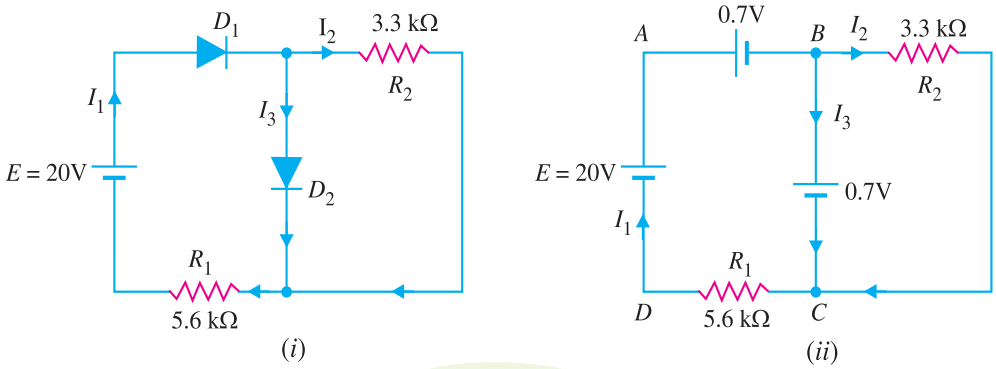


Fig. 6.16

Solution. An inspection of the circuit shown in Fig. 6.16 (*i*) shows that both diodes D_1 and D_2 are forward biased. Using simplified model for the diodes, the circuit shown in Fig. 6.16 (*i*) becomes the one shown in Fig. 6.16 (*ii*). The voltage across R_2 (= 3.3 k Ω) is 0.7V.

$$\therefore \qquad I_2 = \frac{0.7\ \text{V}}{3.3\ \text{k}\Omega} = \mathbf{0.212\ mA}$$

Applying Kirchhoff's voltage law to loop *ABCDA* in Fig. 6.16 (*ii*), we have,

$$-0.7 - 0.7 - I_1 R_1 + 20 = 0$$

$$\therefore \qquad I_1 = \frac{20 - 0.7 - 0.7}{R_1} = \frac{18.6\ \text{V}}{5.6\ \text{k}\Omega} = \mathbf{3.32\ mA}$$

Now $\qquad I_1 = I_2 + I_3$

$$\therefore \qquad I_3 = I_1 - I_2 = 3.32 - 0.212 = \mathbf{3.108\ mA}$$

Example 6.10. *Determine if the diode (ideal) in Fig. 6.17 (i) is forward biased or reverse biased.*

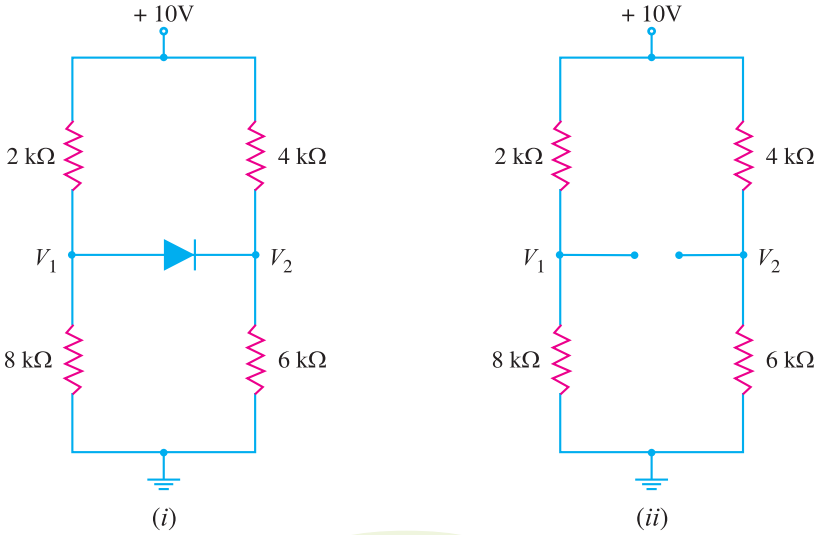


Fig. 6.17

Solution. Let us assume that diode in Fig. 6.17 (*i*) is *OFF i.e.* it is reverse biased. The circuit then becomes as shown in Fig. 6.17 (*ii*). Referring to Fig. 6.17 (*ii*), we have,

$$V_1 = \frac{10\ \text{V}}{2\ \text{k}\Omega + 8\ \text{k}\Omega} \times 8\ \text{k}\Omega = 8\text{V}$$

$$V_2 = \frac{10\ \text{V}}{4\ \text{k}\Omega + 6\ \text{k}\Omega} \times 6\ \text{k}\Omega = 6\text{V}$$

$\therefore$ Voltage across diode $= V_1 - V_2 = 8 - 6 = 2\text{V}$

Now $V_1 - V_2 = 2\text{V}$ is enough voltage to make the diode *forward biased*. Therefore, our initial assumption was wrong.

Example 6.11. *Determine the state of diode for the circuit shown in Fig. 6.18 (i) and find I_D and V_D. Assume simplified model for the diode.*

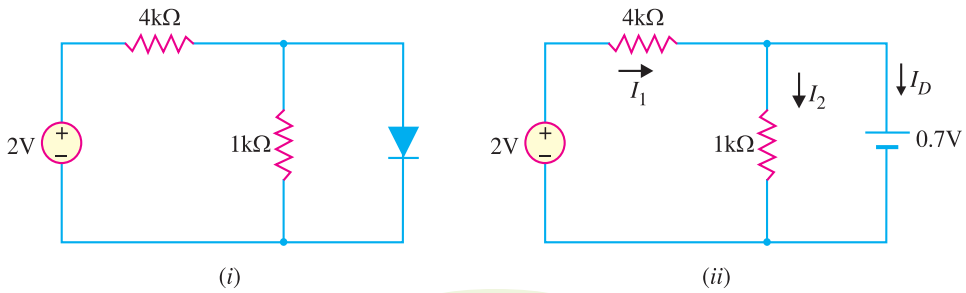


Fig. 6.18

Solution. Let us assume that the diode is *ON*. Therefore, we can replace the diode with a 0.7V battery as shown in Fig. 6.18 (*ii*). Referring to Fig. 6.18 (*ii*), we have,

$$I_1 = \frac{(2 - 0.7)\ \text{V}}{4\ \text{k}\Omega} = \frac{1.3\ \text{V}}{4\ \text{k}\Omega} = 0.325\ \text{mA}$$

$$I_2 = \frac{0.7\ \text{V}}{1\ \text{k}\Omega} = 0.7\ \text{mA}$$

Now $I_D = I_1 - I_2 = 0.325 - 0.7 = -0.375\ \text{mA}$

Since the diode current is negative, the diode must be **OFF** and the true value of diode current is I_D = **0 mA**. Our initial assumption was wrong. In order to analyse the circuit properly, we should replace the diode in Fig. 6.18 (*i*) with an open circuit as shown in Fig. 6.19. The voltage V_D across the diode is

$$V_D = \frac{2\ \text{V}}{1\ \text{k}\Omega + 4\ \text{k}\Omega} \times 1\ \text{k}\Omega = \mathbf{0.4V}$$

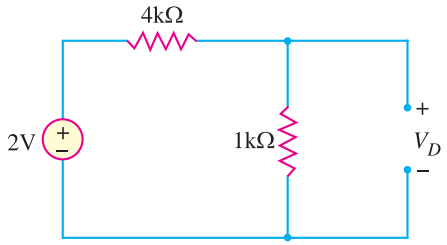


Fig. 6.19

We know that 0.7V is required to turn *ON* the diode. Since V_D is only 0.4V, the answer confirms that the diode is *OFF*.

6.6 Important Terms

While discussing the diode circuits, the reader will generally come across the following terms :

(*i*) Forward current. It is the current flowing through a forward biased diode. Every diode has a maximum value of forward current which it can safely carry. If this value is exceeded, the diode may be destroyed due to excessive heat. For this reason, the manufacturers' data sheet specifies the maximum forward current that a diode can handle safely.

(*ii*) Peak inverse voltage. *It is the maximum reverse voltage that a diode can withstand without destroying the junction.*

If the reverse voltage across a diode exceeds this value, the reverse current increases sharply and breaks down the junction due to excessive heat. Peak inverse voltage is extremely important when diode is used as a rectifier. In rectifier service, it has to be ensured that reverse voltage across the diode does not exceed its PIV during the negative half-cycle of input a.c. voltage. As a matter of fact, PIV consideration is generally the deciding factor in diode rectifier circuits. The peak inverse voltage may be between 10V and 10 kV depending upon the type of diode.

(*iii*) Reverse current or leakage current. It is the current that flows through a reverse biased diode. This current is due to the minority carriers. Under normal operating voltages, the reverse current is quite small. Its value is extremely small (< 1μ A) for silicon diodes but it is appreciable (≃ 100 μA) for germanium diodes.

It may be noted that the reverse current is usually very small as compared with forward current. For example, the forward current for a typical diode might range upto 100 mA while the reverse current might be only a few μA—a ratio of many thousands between forward and reverse currents.

6.7 Crystal Diode Rectifiers

For reasons associated with economics of generation and transmission, the electric power available is usually an a.c. supply. The supply voltage varies sinusoidally and has a frequency of 50 Hz. It is used for lighting, heating and electric motors. But there are many applications (*e.g.* electronic circuits) where d.c. supply is needed. When such a d.c. supply is required, the mains a.c. supply is rectified by using crystal diodes. The following two rectifier circuits can be used :

(*i*) Half-wave rectifier (*ii*) Full-wave rectifier

6.8 Half-Wave Rectifier

In half-wave rectification, the rectifier conducts current only during the positive half-cycles of input a.c. supply. The negative half-cycles of a.c. supply are suppressed *i.e.* during negative half-cycles, no current is conducted and hence no voltage appears across the load. Therefore, current always flows in one direction (*i.e.* d.c.) through the load though after every half-cycle.

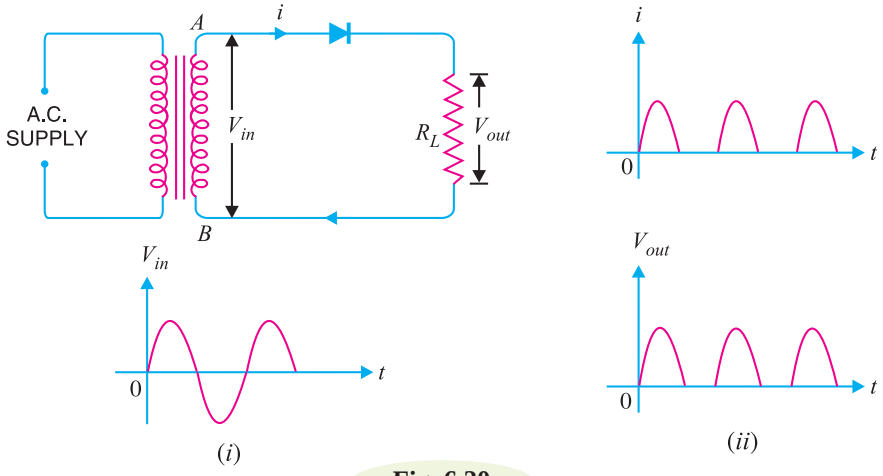


Fig. 6.20

Circuit details. Fig. 6.20 shows the circuit where a single crystal diode acts as a half-wave rectifier. The a.c. supply to be rectified is applied in series with the diode and load resistance R_L. Generally, a.c. supply is given through a transformer. The use of transformer permits two advantages. Firstly, it allows us to step up or step down the a.c. input voltage as the situation demands. Secondly, the transformer isolates the rectifier circuit from power line and thus reduces the risk of electric shock.

Operation. The a.c. voltage across the secondary winding *AB* changes polarities after every half-cycle. During the positive half-cycle of input a.c. voltage, end *A* becomes positive *w.r.t.* end *B*. This makes the diode forward biased and hence it conducts current. During the negative half-cycle, end *A* is negative *w.r.t.* end *B*. Under this condition, the diode is reverse biased and it conducts no current. Therefore, current flows through the diode during positive half-cycles of input a.c. voltage only ; it is blocked during the negative half-cycles [See Fig. 6.20 (*ii*)]. In this way, current flows through load R_L always in the same direction. Hence d.c. output is obtained across R_L. It may be noted that output across the load is pulsating d.c. These pulsations in the output are further smoothened with the help of *filter circuits* discussed later.

Disadvantages : The main disadvantages of a half-wave rectifier are :

(*i*) The pulsating current in the load contains alternating component whose basic frequency is equal to the supply frequency. Therefore, an elaborate filtering is required to produce steady direct current.

(*ii*) The a.c. supply delivers power only half the time. Therefore, the output is low.

6.9 Output Frequency of Half-Wave Rectifier

The output frequency of a half-wave rectifier is equal to the input frequency (50 Hz). Recall how a complete cycle is defined. A waveform has a complete cycle when it repeats the same wave pattern over a given time. Thus in Fig. 6.21 (*i*), the a.c. input voltage repeats the same wave pattern over 0° – 360°, 360° – 720° and so on. In Fig. 6.21 (*ii*), the output waveform also repeats the same wave pattern over 0° – 360°, 360° – 720° and so on. This means that when input a.c. completes one cycle, the output half-wave rectified wave also completes one cycle. In other words, the output frequency is equal to the input frequency *i.e.*

$$f_{out} = f_{in}$$

For example, if the input frequency of sine wave applied to a half-wave rectifier is 100 Hz, then frequency of the output wave will also be 100 Hz.

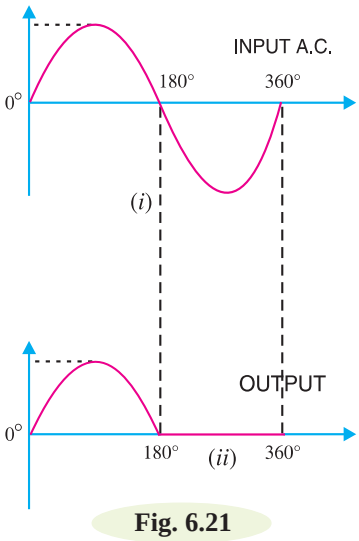


Fig. 6.21

6.10 Efficiency of Half-Wave Rectifier

The ratio of d.c. power output to the applied input a.c. power is known as **rectifier efficiency** *i.e.*

$$\text{Rectifier efficiency, } \eta = \frac{\text{d.c. power output}}{\text{Input a.c. power}}$$

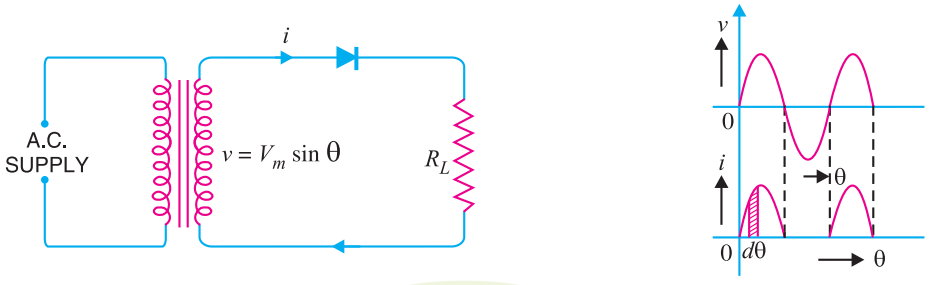


Fig. 6.22

Consider a half-wave rectifier shown in Fig. 6.22. Let $v = V_m \sin \theta$ be the alternating voltage that appears across the secondary winding. Let r_f and R_L be the diode resistance and load resistance respectively. The diode conducts during positive half-cycles of a.c. supply while no current conduction takes place during negative half-cycles.

d.c. power. The output current is pulsating direct current. Therefore, in order to find d.c. power, average current has to be found out.

$$*I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i\, d\theta = \frac{1}{2\pi}\int_0^{\pi} \frac{V_m \sin\theta}{r_f + R_L}\, d\theta$$

$$= \frac{V_m}{2\pi(r_f + R_L)}\int_0^{\pi} \sin\theta\, d\theta = \frac{V_m}{2\pi(r_f + R_L)}[-\cos\theta]_0^{\pi}$$

$$= \frac{V_m}{2\pi(r_f + R_L)} \times 2 = \frac{V_m}{(r_f + R_L)} \times \frac{1}{\pi}$$

$$= **\frac{I_m}{\pi} \qquad \left[\because I_m = \frac{V_m}{(r_f + R_L)}\right]$$

$$\therefore \quad \text{d.c. power, } P_{dc} = I_{dc}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L \qquad ...(i)$$

a.c. power input : The a.c. power input is given by :

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a half-wave rectified wave, $I_{rms} = I_m/2$

$$\therefore \quad P_{ac} = \left(\frac{I_m}{2}\right)^2 \times (r_f + R_L) \qquad ...(ii)$$

$$\therefore \quad \text{Rectifier efficiency} = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2 (r_f + R_L)}$$

$$= \frac{0.406\, R_L}{r_f + R_L} = \frac{0.406}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ Max. rectifier efficiency = 40.6%

This shows that in half-wave rectification, a maximum of 40.6% of a.c. power is converted into d.c. power.

Example 6.12. *The applied input a.c. power to a half-wave rectifier is 100 watts. The d.c. output power obtained is 40 watts.*

(*i*) *What is the rectification efficiency ?*

(*ii*) *What happens to remaining 60 watts ?*

Solution.

(*i*) $\text{Rectification efficiency} = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{40}{100} = 0.4 = \mathbf{40\%}$

(*ii*) 40% efficiency of rectification does not mean that 60% of power is lost in the rectifier circuit. In fact, a crystal diode consumes little power due to its small internal resistance. The 100 W

. . . . . .

* $\text{Average value} = \frac{\text{Area under the curve over a cycle}}{\text{Base}} = \frac{\int_0^{\pi} i\, d\theta}{2\pi}$

** It may be remembered that the *area of one-half cycle of a sinusoidal wave* is twice the peak value. Thus in this case, peak value is I_m and, therefore, area of one-half cycle is $2\, I_m$.

$\therefore \quad I_{av} = I_{dc} = \frac{2\, I_m}{2\pi} = \frac{I_m}{\pi}$

a.c. power is contained as 50 watts in positive half-cycles and 50 watts in negative half-cycles. The 50 watts in the negative half-cycles are not supplied at all. Only 50 watts in the positive half-cycles are converted into 40 watts.

$$\therefore \quad \text{Power efficiency} = \frac{40}{50} \times 100 = 80\%$$

Although 100 watts of a.c. power was supplied, the half-wave rectifier accepted only 50 watts and converted it into 40 watts d.c. power. Therefore, it is appropriate to say that efficiency of rectification is 40% and *not* 80% which is power efficiency.

Example 6.13. *An a.c. supply of 230 V is applied to a half-wave rectifier circuit through a transformer of turn ratio 10 : 1. Find (i) the output d.c. voltage and (ii) the peak inverse voltage. Assume the diode to be ideal.*

Solution.

Primary to secondary turns is

$$\frac{N_1}{N_2} = 10$$

R.M.S. primary voltage = 230 V

$\therefore$ Max. primary voltage is

$$V_{pm} = (\sqrt{2}) \times \text{r.m.s. primary voltage}$$
$$= (\sqrt{2}) \times 230 = 325.3 \text{ V}$$

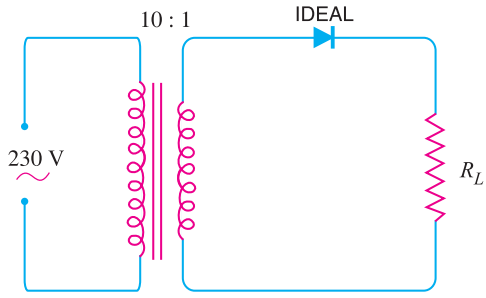


Fig. 6.23

Max. secondary voltage is

$$V_{sm} = V_{pm} \times \frac{N_2}{N_1} = 325.3 \times \frac{1}{10} = 32.53 \text{ V}$$

(i) $$I_{d.c.} = \frac{I_m}{\pi}$$

$\therefore$ $$V_{dc} = \frac{I_m}{\pi} \times R_L = \frac{V_{sm}}{\pi} = \frac{32.53}{\pi} = \mathbf{10.36\ V}$$

(ii) During the negative half-cycle of a.c. supply, the diode is reverse biased and hence conducts no current. Therefore, the maximum secondary voltage appears across the diode.

$\therefore$ Peak inverse voltage = **32.53 V**

Example 6.14. *A crystal diode having internal resistance $r_f = 20\Omega$ is used for half-wave rectification. If the applied voltage $v = 50 \sin \omega t$ and load resistance $R_L = 800\ \Omega$, find :*

(i) I_m, I_{dc}, I_{rms} *(ii) a.c. power input and d.c. power output*

(iii) d.c. output voltage *(iv) efficiency of rectification.*

Solution.

$$v = 50 \sin \omega t$$

$\therefore$ Maximum voltage, $V_m = 50$ V

(i) $$I_m = \frac{V_m}{r_f + R_L} = \frac{50}{20 + 800} = 0.061 \text{ A} = \mathbf{61\ mA}$$

$$I_{dc} = I_m/\pi = 61/\pi = \mathbf{19.4\ mA}$$

$$I_{rms} = I_m/2 = 61/2 = \mathbf{30.5\ mA}$$

(ii) $$\text{a.c. power input} = (I_{rms})^2 \times (r_f + R_L) = \left(\frac{30.5}{1000}\right)^2 \times (20 + 800) = \mathbf{0.763\ watt}$$

$$\text{d.c. power output} = I_{dc}^2 \times R_L = \left(\frac{19.4}{1000}\right)^2 \times 800 = \textbf{0.301 watt}$$

(iii) $$\text{d.c. output voltage} = I_{dc} R_L = 19.4\,\text{mA} \times 800\,\Omega = \textbf{15.52 volts}$$

(iv) $$\text{Efficiency of rectification} = \frac{0.301}{0.763} \times 100 = \textbf{39.5\%}$$

Example 6.15. *A half-wave rectifier is used to supply 50V d.c. to a resistive load of 800 Ω. The diode has a resistance of 25 Ω. Calculate a.c. voltage required.*

Solution.

Output d.c. voltage, $V_{dc} = 50$ V

Diode resistance, $r_f = 25\ \Omega$

Load resistance, $R_L = 800\ \Omega$

Let V_m be the maximum value of a.c. voltage required.

$$\therefore \quad V_{dc} = I_{dc} \times R_L$$

$$= \frac{I_m}{\pi} \times R_L = \frac{V_m}{\pi (r_f + R_L)} \times R_L \qquad \left[\because I_m = \frac{V_m}{r_f + R_L}\right]$$

or $$50 = \frac{V_m}{\pi (25 + 800)} \times 800$$

$$\therefore \quad V_m = \frac{\pi \times 825 \times 50}{800} = \textbf{162 V}$$

Hence a.c. voltage of maximum value 162 V is required.

6.11 Full-Wave Rectifier

In full-wave rectification, current flows through the load in the same direction for both half-cycles of input a.c. voltage. This can be achieved with two diodes working alternately. For the positive half-cycle of input voltage, one diode supplies current to the load and for the negative half-cycle, the other diode does so ; current being always in the same direction through the load. Therefore, a full-wave rectifier utilises both half-cycles of input a.c. voltage to produce the d.c. output. The following two circuits are commonly used for full-wave rectification :

(*i*) Centre-tap full-wave rectifier (*ii*) Full-wave bridge rectifier

6.12 Centre-Tap Full-Wave Rectifier

The circuit employs two diodes D_1 and D_2 as shown in Fig. 6.24. A centre tapped secondary winding AB is used with two diodes connected so that each uses one half-cycle of input a.c. voltage. In other words, diode D_1 utilises the a.c. voltage appearing across the upper half (OA) of secondary winding for rectification while diode D_2 uses the lower half winding OB.

Operation. During the positive half-cycle of secondary voltage, the end A of the secondary winding becomes positive and end B negative. This makes the diode D_1 forward biased and diode D_2 reverse biased. Therefore, diode D_1 conducts while diode D_2 does not. The conventional current flow is through diode D_1, load resistor R_L and the upper half of secondary winding as shown by the dotted arrows. During the negative half-cycle, end A of the secondary winding becomes negative and end B positive. Therefore, diode D_2 conducts while diode D_1 does not. The conventional current flow is through diode D_2, load R_L and lower half winding as shown by solid arrows. Referring to Fig. 6.24, it may be seen that current in the load R_L is *in the same direction* for both half-cycles of input a.c. voltage. Therefore, d.c. is obtained across the load R_L. Also, the polarities of the d.c. output across the load should be noted.

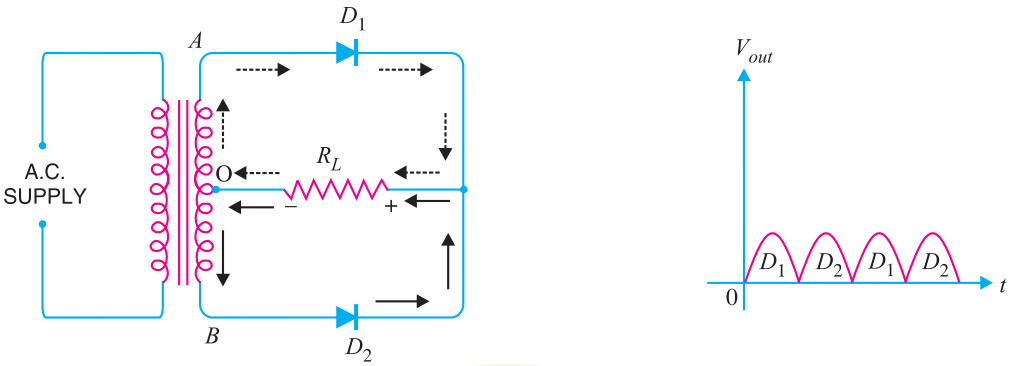


Fig. 6.24

Peak inverse voltage. Suppose V_m is the maximum voltage across the half secondary winding. Fig. 6.25 shows the circuit at the instant secondary voltage reaches its maximum value in the positive direction. At this instant, diode D_1 is conducting while diode D_2 is non-conducting. Therefore, whole of the secondary voltage appears across the non-conducting diode. Consequently, the peak inverse voltage is twice the maximum voltage across the half-secondary winding *i.e.*

$$\text{PIV} = 2\,V_m$$

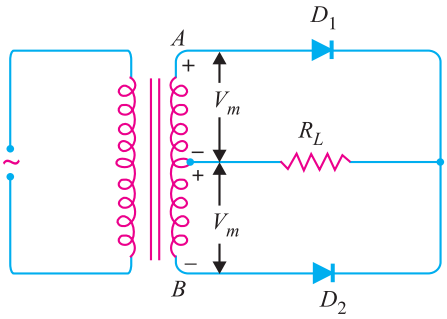


Fig. 6.25

Disadvantages

(i) It is difficult to locate the centre tap on the secondary winding.

(ii) The d.c. output is small as each diode utilises only one-half of the transformer secondary voltage.

(iii) The diodes used must have high peak inverse voltage.

6.13 Full-Wave Bridge Rectifier

The need for a centre tapped power transformer is eliminated in the bridge rectifier. It contains four diodes D_1, D_2, D_3 and D_4 connected to form bridge as shown in Fig. 6.26. The a.c. supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer. Between other two ends of the bridge, the load resistance R_L is connected.

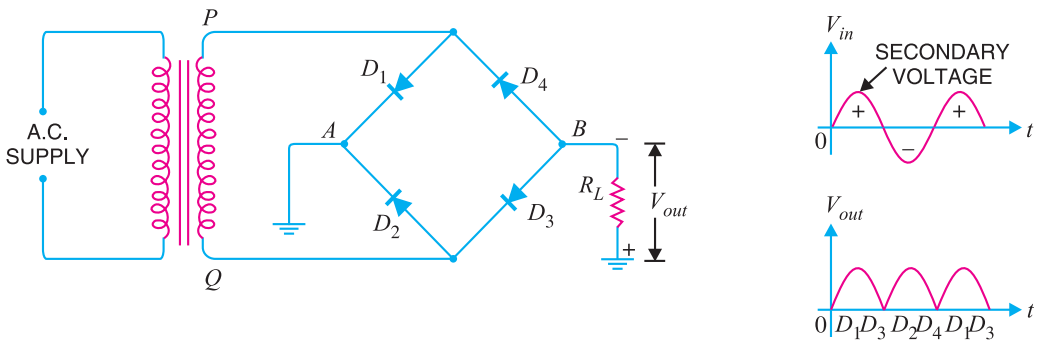


Fig. 6.26

Operation. During the positive half-cycle of secondary voltage, the end P of the secondary winding becomes positive and end Q negative. This makes diodes D_1 and D_3 forward biased while diodes D_2 and D_4 are reverse biased. Therefore, only diodes D_1 and D_3 conduct. These two diodes will be in series through the load R_L as shown in Fig. 6.27 (*i*). The conventional current flow is shown by dotted arrows. It may be seen that current flows from A to B through the load R_L .

During the negative half-cycle of secondary voltage, end P becomes negative and end Q positive. This makes diodes D_2 and D_4 forward biased whereas diodes D_1 and D_3 are reverse biased. Therefore, only diodes D_2 and D_4 conduct. These two diodes will be in series through the load R_L as shown in Fig. 6.27 (*ii*). The current flow is shown by the solid arrows. It may be seen that again current flows from A to B through the load *i.e.* in the same direction as for the positive half-cycle. Therefore, d.c. output is obtained across load R_L.

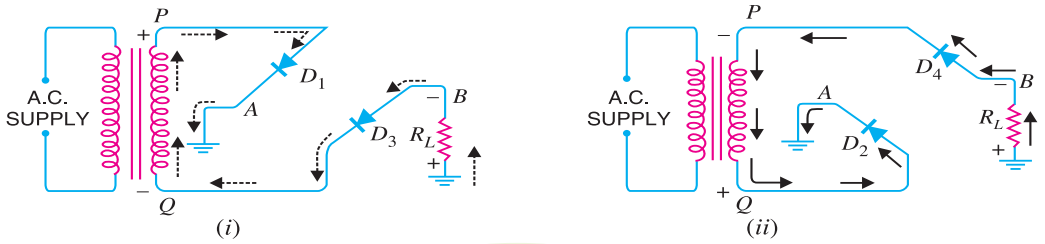


Fig. 6.27

Peak inverse voltage. The peak inverse voltage (PIV) of each diode is equal to the maximum secondary voltage of transformer. Suppose during positive half cycle of input a.c., end P of secondary is positive and end Q negative. Under such conditions, diodes D_1 and D_3 are forward biased while diodes D_2 and D_4 are reverse biased. Since the diodes are considered ideal, diodes D_1 and D_3 can be replaced by wires as shown in Fig. 6.28 (*i*). This circuit is the same as shown in Fig. 6.28 (*ii*).

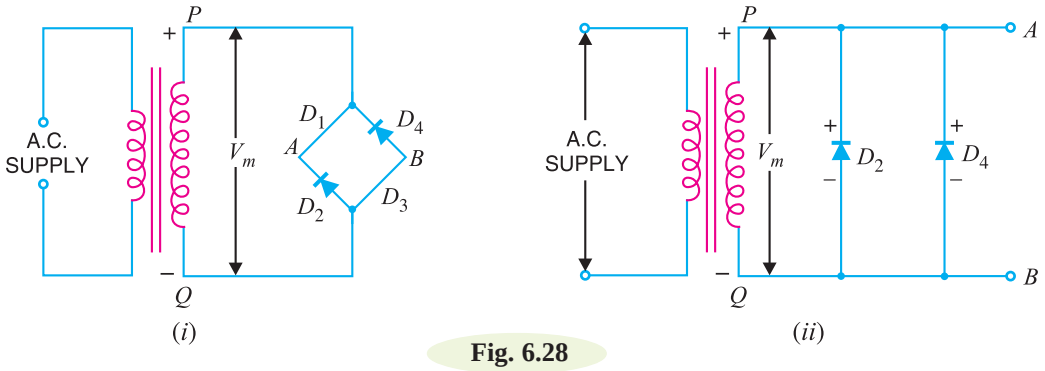


Fig. 6.28

Referring to Fig. 6.28 (*ii*), it is clear that two reverse biased diodes (*i.e.*, D_2 and D_4) and the secondary of transformer are in parallel. Hence PIV of each diode (D_2 and D_4) is equal to the maximum voltage (V_m) across the secondary. Similarly, during the next half cycle, D_2 and D_4 are forward biased while D_1 and D_3 will be reverse biased. It is easy to see that reverse voltage across D_1 and D_3 is equal to V_m.

Advantages

(*i*) The need for centre-tapped transformer is eliminated.

(*ii*) The output is twice that of the centre-tap circuit for the same secondary voltage.

(*iii*) The PIV is one-half that of the centre-tap circuit (for same d.c. output).

Disadvantages

(*i*) It requires four diodes.

(ii) As during each half-cycle of a.c. input two diodes that conduct are in series, therefore, voltage drop in the internal resistance of the rectifying unit will be twice as great as in the centre tap circuit. This is objectionable when secondary voltage is small.

6.14 Output Frequency of Full-Wave Rectifier

The output frequency of a full-wave rectifier is double the input frequency. Remember that a wave has a complete cycle when it repeats the same pattern. In Fig. 6.29 (*i*), the input a.c. completes one cycle from 0° – 360°. However, the full-wave rectified wave completes 2 cycles in this period [See Fig. 6.29 (*ii*)]. Therefore, output frequency is twice the input frequency *i.e.*

$$f_{out} = 2\, f_{in}$$

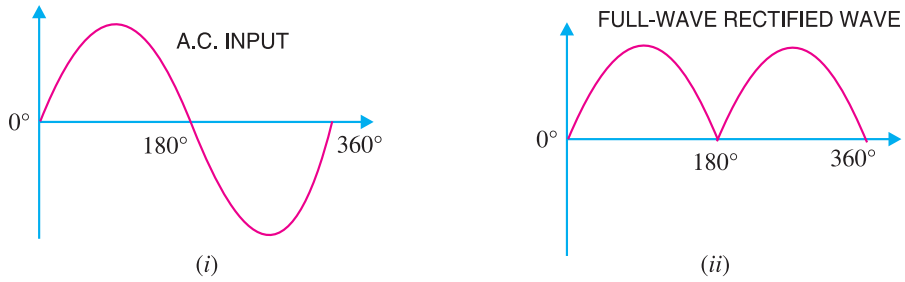


Fig. 6.29

For example, if the input frequency to a full-wave rectifier is 100 Hz, then the output frequency will be 200 Hz.

6.15 Efficiency of Full-Wave Rectifier

Fig. 6.30 shows the process of full-wave rectification. Let $v = V_m \sin \theta$ be the a.c. voltage to be rectified. Let r_f and R_L be the diode resistance and load resistance respectively. Obviously, the rectifier will conduct current through the load in the same direction for both half-cycles of input a.c. voltage. The instantaneous current i is given by :

$$i = \frac{v}{r_f + R_L} = \frac{V_m \sin \theta}{r_f + R_L}$$

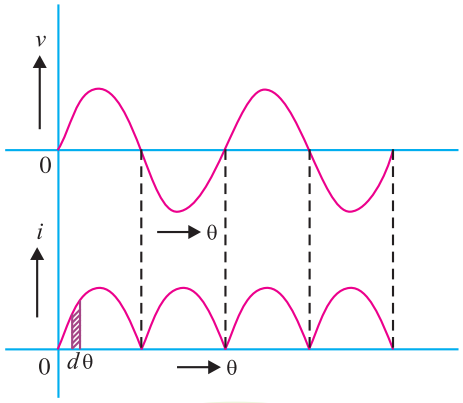


Fig. 6.30

d.c. output power. The output current is pulsating direct current. Therefore, in order to find the d.c. power, average current has to be found out. From the elementary knowledge of electrical engineering,

$$I_{dc} = \frac{2I_m}{\pi}$$

$\therefore$ d.c. power output, $P_{dc} = I_{dc}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$ ...(*i*)

a.c. input power. The a.c. input power is given by :

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

For a full-wave rectified wave, we have,

$$I_{rms} = I_m/\sqrt{2}$$

$\therefore$ $$P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)$$ ... (*ii*)

$\therefore$ Full-wave rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (r_f + R_L)}$$

$$= \frac{8}{\pi^2} \times \frac{R_L}{(r_f + R_L)} = \frac{0.812\ R_L}{r_f + R_L} = \frac{0.812}{1 + \frac{r_f}{R_L}}$$

The efficiency will be maximum if r_f is negligible as compared to R_L.

$\therefore$ Maximum efficiency = 81.2%

This is double the efficiency due to half-wave rectifier. Therefore, a full-wave rectifier is twice as effective as a half-wave rectifier.

Example 6.16. *A full-wave rectifier uses two diodes, the internal resistance of each diode may be assumed constant at 20 Ω. The transformer r.m.s. secondary voltage from centre tap to each end of secondary is 50 V and load resistance is 980 Ω. Find :*

(*i*) *the mean load current* (*ii*) *the r.m.s. value of load current*

Solution.

$$r_f = 20\ \Omega, \quad R_L = 980\ \Omega$$

Max. a.c. voltage, $V_m = 50 \times \sqrt{2} = 70.7$ V

Max. load current, $I_m = \frac{V_m}{r_f + R_L} = \frac{70.7\ \text{V}}{(20 + 980)\ \Omega} = 70.7$ mA

(*i*) Mean load current, $I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 70.7}{\pi}$ = **45 mA**

(*ii*) R.M.S. value of load current is

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{70.7}{\sqrt{2}} \overrightarrow{AB} = \textbf{50 mA}$$

Example 6.17. *In the centre-tap circuit shown in Fig. 6.31, the diodes are assumed to be ideal i.e. having zero internal resistance. Find :*

(*i*) *d.c. output voltage* (*ii*) *peak inverse voltage* (*iii*) *rectification efficiency.*

Solution.

Primary to secondary turns, $N_1/N_2 = 5$

R.M.S. primary voltage = 230 V

∴ R.M.S. secondary voltage

$= 230 \times (1/5) = 46$ V

Maximum voltage across secondary

$= 46 \times \sqrt{2} = 65$ V

Maximum voltage across half secondary winding is

$V_m = 65/2 = 32.5$ V

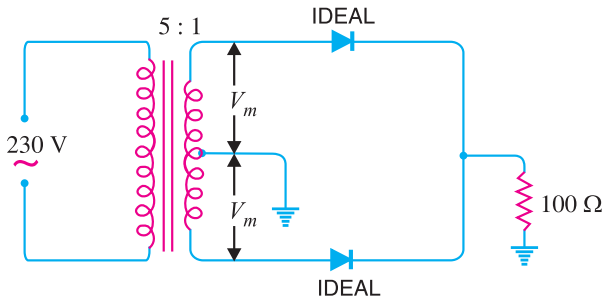


Fig. 6.31

(i) Average current, $I_{dc} = \dfrac{2V_m}{\pi R_L} = \dfrac{2 \times 32.5}{\pi \times 100} = 0.207$ A

∴ d.c. output voltage, $V_{dc} = I_{dc} \times R_L = 0.207 \times 100 =$ **20.7 V**

(ii) The peak inverse voltage is equal to the maximum secondary voltage, *i.e.*

$PIV =$ **65 V**

(iii) Rectification efficiency $= \dfrac{0.812}{1 + \dfrac{r_f}{R_L}}$

Since $r_f = 0$

∴ Rectification efficiency = **81.2 %**

Example 6.18. *In the bridge type circuit shown in Fig. 6.32, the diodes are assumed to be ideal. Find : (i) d.c. output voltage (ii) peak inverse voltage (iii) output frequency. Assume primary to secondary turns to be 4.*

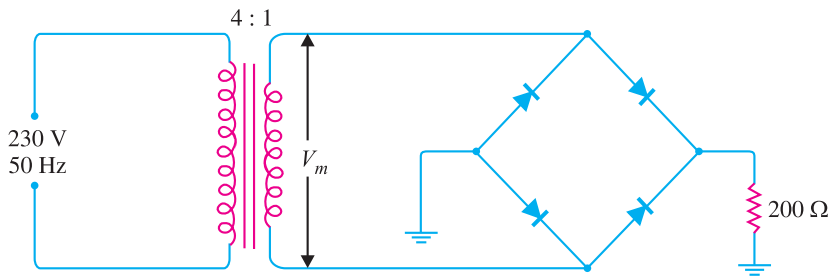


Fig. 6.32

Solution.

Primary/secondary turns, $N_1/N_2 = 4$

R.M.S. primary voltage = 230 V

∴ R.M.S. secondary voltage $= 230\ (N_2/N_1) = 230 \times (1/4) = 57.5$ V

Maximum voltage across secondary is

$V_m = 57.5 \times \sqrt{2} = 81.3$ V

(i) Average current, $I_{dc} = \dfrac{2V_m}{\pi R_L} = \dfrac{2 \times 81.3}{\pi \times 200} = 0.26$ A

∴ d.c. output voltage, $V_{dc} = I_{dc} \times R_L = 0.26 \times 200 =$ **52 V**

(*ii*) The peak inverse voltage is equal to the maximum secondary voltage *i.e.*

$$PIV = \mathbf{81.3\ V}$$

(*iii*) In full-wave rectification, there are two output pulses for each complete cycle of the input a.c. voltage. Therefore, the output frequency is twice that of the a.c. supply frequency *i.e.*

$$f_{out} = 2 \times f_{in} = 2 \times 50 = \mathbf{100\ Hz}$$

Example 6.19. *Fig. 6.33 (i) and Fig. 6.33 (ii) show the centre-tap and bridge type circuits having the same load resistance and transformer turn ratio. The primary of each is connected to 230V, 50 Hz supply.*

(*i*) *Find the d.c. voltage in each case.*

(*ii*) *PIV for each case for the same d.c. output. Assume the diodes to be ideal.*

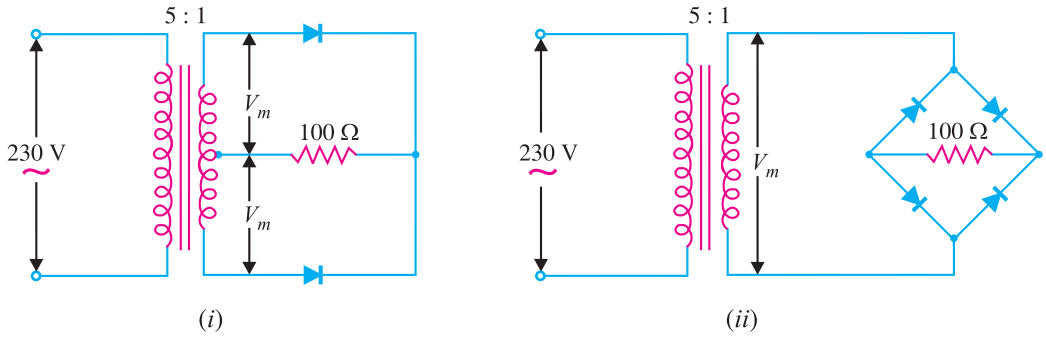


Fig. 6.33

Solution.

(*i*) D.C. output voltage

Centre-tap circuit

$$\text{R.M.S. secondary voltage} = 230 \times 1/5 = 46\ \text{V}$$

$$\text{Max. voltage across secondary} = 46 \times \sqrt{2} = 65\ \text{V}$$

Max. voltage appearing across half secondary winding is

$$V_m = 65/2 = 32.5\ \text{V}$$

$$\text{Average current, } I_{dc} = \frac{2V_m}{\pi R_L}$$

$$\text{D.C. output voltage, } V_{dc} = I_{dc} \times R_L = \frac{2V_m}{\pi R_L} \times R_L$$

$$= \frac{2V_m}{\pi} = \frac{2 \times 32.5}{\pi} = \mathbf{20.7\ V}$$

Bridge Circuit

$$\text{Max. voltage across secondary, } V_m = 65\ \text{V}$$

$$\text{D.C. output voltage, } V_{dc} = I_{dc} R_L = \frac{2V_m}{\pi R_L} \times R_L = \frac{2V_m}{\pi} = \frac{2 \times 65}{\pi} = \mathbf{41.4\ V}$$

This shows that for the same secondary voltage, the d.c. output voltage of bridge circuit is twice that of the centre-tap circuit.

(*ii*) PIV for same d.c. output voltage

The d.c. output voltage of the two circuits will be the same if V_m (*i.e.* max. voltage utilised by each circuit for conversion into d.c.) is the same. For this to happen, the turn ratio of the transformers should be as shown in Fig. 6.34.

Centre-tap circuit

R.M.S. secondary voltage = $230 \times 1/5 = 46$ V

Max. voltage across secondary = $46 \times \sqrt{2} = 65$ V

Max. voltage across half secondary winding is

$$V_m = 65/2 = 32.5 \text{ V}$$

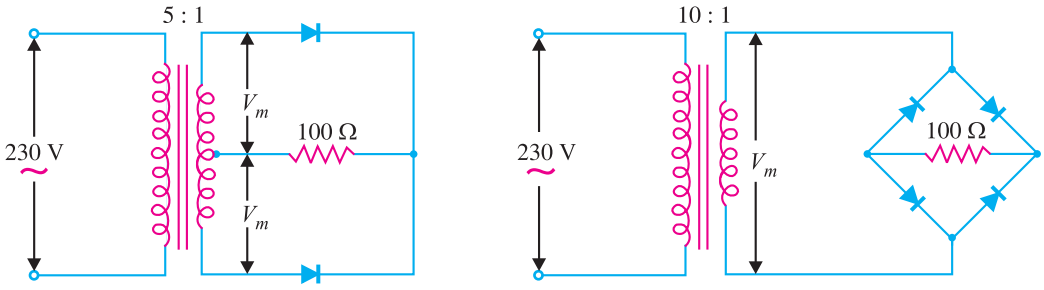


Fig. 6.34

$\therefore$ $PIV = 2\,V_m = 2 \times 32.5 =$ **65 V**

Bridge type circuit

R.M.S. secondary voltage = $230 \times 1/10 = 23$ V

Max. voltage across secondary, $V_m = 23 \times \sqrt{2} = 32.5$ V

$\therefore$ $PIV = V_m =$ **32.5 V**

This shows that for the same d.c. output voltage, *PIV* of bridge circuit is half that of centre-tap circuit. This is a distinct advantage of bridge circuit.

Example 6.20. *The four diodes used in a bridge rectifier circuit have forward resistances which may be considered constant at 1Ω and infinite reverse resistance. The alternating supply voltage is 240 V r.m.s. and load resistance is 480 Ω. Calculate (i) mean load current and (ii) power dissipated in each diode.*

Solution.

Max. a.c. voltage, $V_m = 240 \times \sqrt{2}$ V

(i) At any instant in the bridge rectifier, two diodes in series are conducting. Therefore, total circuit resistance = $2\,r_f + R_L$.

$$\text{Max. load current, } I_m = \frac{V_m}{2\,r_f + R_L} = \frac{240 \times \sqrt{2}}{2 \times 1 + 480} = 0.7 \text{ A}$$

$\therefore$ $$\text{Mean load current, } I_{dc} = \frac{2\,I_m}{\pi} = \frac{2 \times 0.7}{\pi} = \textbf{0.45 A}$$

(ii) Since each diode conducts only half a cycle, diode r.m.s. current is :

$$I_{r.m.s.} = I_m/2 = 0.7/2 = 0.35 \text{ A}$$

Power dissipated in each diode = $I^2_{r.m.s.} \times r_f = (0.35)^2 \times 1 =$ **0.123 W**

Example 6.21. *The bridge rectifier shown in Fig. 6.35 uses silicon diodes. Find (i) d.c. output*

voltage (ii) d.c. output current. Use simplified model for the diodes.

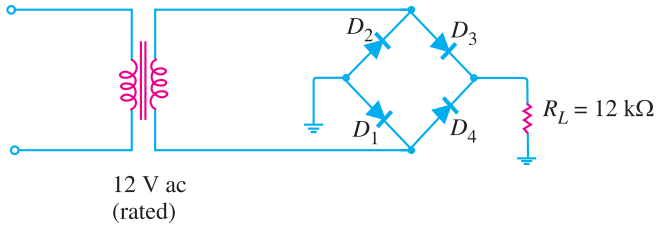


Fig. 6.35

Solution. The conditions of the problem suggest that the a.c voltage across transformer secondary is 12V r.m.s.

∴ Peak secondary voltage is

$$V_{s\,(pk)} = 12 \times \sqrt{2} = 16.97 \text{ V}$$

(*i*) At any instant in the bridge rectifier, two diodes in series are conducting.

∴ Peak output voltage is

$$V_{out\,(pk)} = 16.97 - 2\,(0.7) = 15.57 \text{ V}$$

∴ Average (or d.c.) output voltage is

$$V_{av} = V_{dc} = \frac{2\,V_{out\,(pk)}}{\pi} = \frac{2 \times 15.57}{\pi} = \mathbf{9.91V}$$

(*ii*) Average (or d.c.) output current is

$$I_{av} = \frac{V_{av}}{R_L} = \frac{9.91\text{V}}{12\ \text{k}\Omega} = \mathbf{825.8\ \mu A}$$

6.16 Faults in Centre-Tap Full-Wave Rectifier

The faults in a centre-tap full-wave rectifier may occur in the transformer or rectifier diodes. Fig. 6.36 shows the circuit of a centre-tap full-wave rectifier. A fuse is connected in the primary of the transformer for protection purposes.

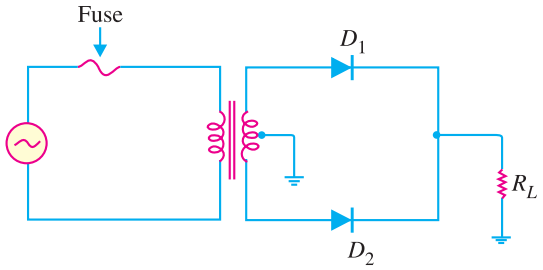


Fig. 6.36

We can divide the rectifier faults into two classes viz.

1. Faults in transformer **2.** Faults in rectifier diodes

1. Faults in Transformer. The transformer in a rectifier circuit can develop the following faults :

(*i*) A shorted primary or secondary winding.

(*ii*) An open primary or secondary winding.

(*iii*) A short between the primary or secondary winding and the transformer frame.

(*i*) In most cases, a **shorted primary** or **shorted secondary** will cause the fuse in the primary

to blow. If the fuse does not blow, the d.c. output from the rectifier will be extremely low and the transformer itself will be very hot.

(ii) When the **primary** or **secondary winding of the transformer opens**, the output from the rectifier will drop to zero. In this case, the primary fuse will not blow. If you believe that either transformer winding is open, a simple resistance check will verify your doubt. If either winding reads a very high resistance, the winding is open.

(iii) If **either winding shorts to the transformer casing**, the primary fuse will blow. This fault can be checked by measuring the resistances from the winding leads to the transformer casing. A low resistance measurement indicates that a winding-to-case short exists.

2. Faults in Rectifier Diodes. If a fault occurs in a rectifier diode, the circuit conditions will indicate the type of fault.

(i) If **one diode in the centre-tap full-wave rectifier is shorted**, the primary fuse will blow. The reason is simple. Suppose diode D_2 in Fig. 6.36 is shorted. Then diode D_2 will behave as a wire. When diode D_1 is forward biased, the transformer secondary will be shorted through D_1. This will cause excessive current to flow in the secondary (and hence in the primary), causing the primary fuse to blow.

(ii) If **one diode in the centre-tap full-wave rectifier opens**, the output from the rectifier will resemble the output from a half-wave rectifier. The remedy is to replace the diode.

Bridge Rectifier Faults. The transformer faults and their remedies for bridge rectifier circuits are the same as for centre-tap full-wave rectifier. Again symptoms for shorted and open diodes in the bridge rectifier are the same as those for the centre-tap circuit. In the case of bridge circuit, you simply have more diodes that need to be tested.

6.17 Nature of Rectifier Output

It has already been discussed that the output of a rectifier is pulsating d.c. as shown in Fig. 6.37. In fact, if such a waveform is carefully analysed, it will be found that it contains a d.c. component and an a.c. component. The a.c. component is responsible for the *pulsations in the wave. The reader may wonder how a pulsating d.c. voltage can have an a.c. component when the voltage never becomes negative. The answer is that any wave which varies in a regular manner has an a.c. component.

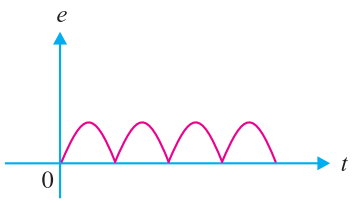


Fig. 6.37

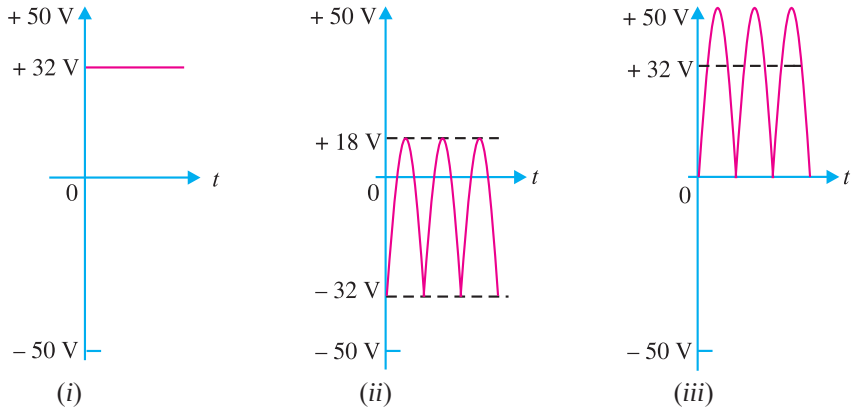


Fig. 6.38

* Means changing output voltage.


Rectifier

The fact that a pulsating d.c. contains both d.c. and a.c. components can be beautifully illustrated by referring to Fig. 6.38. Fig. 6.38 (*i*) shows a pure d.c. component, whereas Fig. 6.38 (*ii*) shows the *a.c. component. If these two waves are added together, the resulting wave will be as shown in Fig. 6.38 (*iii*). It is clear that the wave shown in Fig. 6.38 (*iii*) never becomes negative, although it contains both a.c. and d.c. components. The striking resemblance between the rectifier output wave shown in Fig. 6.37 and the wave shown in Fig. 6.38 (*iii*) may be noted.

It follows, therefore, that a pulsating output of a rectifier contains a d.c. component and an a.c. component.

6.18 Ripple Factor

The output of a rectifier consists of a d.c. component and an a.c. component (also known as *ripple*). The a.c. component is undesirable and accounts for the pulsations in the rectifier output. The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output ; the smaller this component, the more effective is the rectifier.

The ratio of r.m.s. value of a.c. component to the d.c. component in the rectifier output is known as **ripple factor** *i.e.*

$$\text{Ripple factor} = \frac{\text{r.m.s. value of a.c component}}{\text{value of d.c. component}} = \frac{I_{ac}}{I_{dc}}$$

Therefore, ripple factor is very important in deciding the effectiveness of a rectifier. The smaller the ripple factor, the lesser the effective a.c. component and hence more effective is the rectifier.

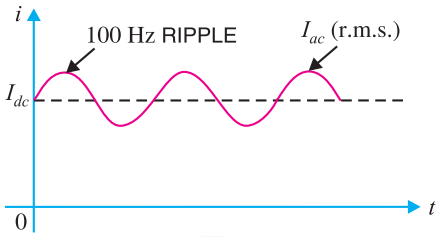


Fig. 6.39

Mathematical analysis. The output current of a rectifier contains d.c. as well as a.c. component. The undesired a.c. component has a frequency of 100 Hz (*i.e.* double the supply frequency 50 Hz) and is called the *ripple* (See Fig. 6.39). It is a fluctuation superimposed on the d.c. component.

By definition, the effective (*i.e.* r.m.s.) value of total load current is given by :

$$I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2}$$

or
$$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

Dividing throughout by I_{dc}, we get,

$$\frac{I_{ac}}{I_{dc}} = \frac{1}{I_{dc}}\sqrt{I_{rms}^2 - I_{dc}^2}$$

But I_{ac}/I_{dc} is the ripple factor.

$$\therefore \quad \text{Ripple factor} = \frac{1}{I_{dc}}\sqrt{I_{rms}^2 - I_{dc}^2} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

(*i*) For half-wave rectification. In half-wave rectification,

$$I_{rms} = I_m/2 \quad ; \quad I_{dc} = I_m/\pi$$

* Although the a.c. component is not a sine-wave, yet it is alternating one.

$$\therefore \quad \text{Ripple factor} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = 1.21$$

It is clear that a.c. component exceeds the d.c. component in the output of a half-wave rectifier. This results in greater pulsations in the output. Therefore, half-wave rectifier is ineffective for conversion of a.c. into d.c.

***(ii)* For full-wave rectification.** In full-wave rectification,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad ; \quad I_{dc} = \frac{2I_m}{\pi}$$

$$\therefore \quad \text{Ripple factor} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = 0.48$$

$$i.e. \quad \frac{\text{effective a.c. component}}{\text{d.c. component}} = 0.48$$

This shows that in the output of a full-wave rectifier, the d.c. component is more than the a.c. component. Consequently, the pulsations in the output will be less than in half-wave rectifier. For this reason, full-wave rectification is invariably used for conversion of a.c. into d.c.

Example 6.22. *A power supply A delivers 10 V dc with a ripple of 0.5 V r.m.s. while the power supply B delivers 25 V dc with a ripple of 1 mV r.m.s. Which is better power supply ?*

Solution. The lower the ripple factor of a power supply, the better it is.

For power supply A

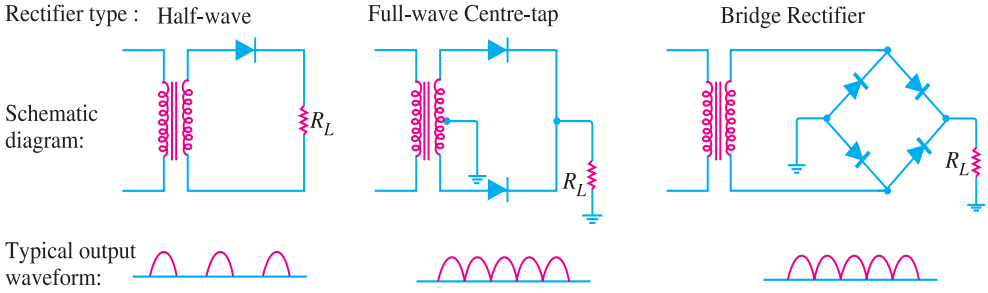
$$\text{Ripple factor} = \frac{V_{ac(r.m.s.)}}{V_{dc}} = \frac{0.5}{10} \times 100 = 5\%$$

For power supply B

$$\text{Ripple factor} = \frac{V_{ac(r.m.s.)}}{V_{dc}} = \frac{0.001}{25} \times 100 = 0.004\%$$

Clearly, power supply *B* is better.

6.19 Comparison of Rectifiers



S. No.	Particulars	Half-wave	Centre-tap	Bridge type
1	No. of diodes	1	2	4
2	Transformer necessary	no	yes	no
3	Max. efficiency	40.6%	81.2%	81.2%
4	Ripple factor	1.21	0.48	0.48
5	Output frequency	f_{in}	$2f_{in}$	$2f_{in}$
6	Peak inverse voltage	V_m	$2V_m$	V_m

A comparison among the three rectifier circuits must be made very judiciously. Although bridge circuit has some disadvantages, it is the best circuit from the viewpoint of overall performance. When cost of the transformer is the main consideration in a rectifier assembly, we invariably use the bridge circuit. This is particularly true for large rectifiers which have a low-voltage and a high-current rating.

6.20 Filter Circuits

Generally, a rectifier is required to produce pure d.c. supply for using at various places in the electronic circuits. However, the output of a rectifier has pulsating *character *i.e.* it contains a.c. and d.c. components. The a.c. component is undesirable and must be kept away from the load. To do so, a *filter circuit* is used which removes (or *filters out*) the a.c. component and allows only the d.c. component to reach the load.

A **filter circuit** *is a device which removes the a.c. component of rectifier output but allows the d.c. component to reach the load.*

Obviously, a filter circuit should be installed between the rectifier and the load as shown in Fig. 6.40. A filter circuit is generally a combination of inductors (L) and capacitors (C). The filtering action of L and C depends upon the basic electrical principles. A capacitor passes a.c. readily but does not **pass d.c. at all. On the other hand, an inductor †opposes a.c. but allows d.c. to pass through it. It then becomes clear that suitable network of L and C can effectively remove the a.c. component, allowing the d.c. component to reach the load.

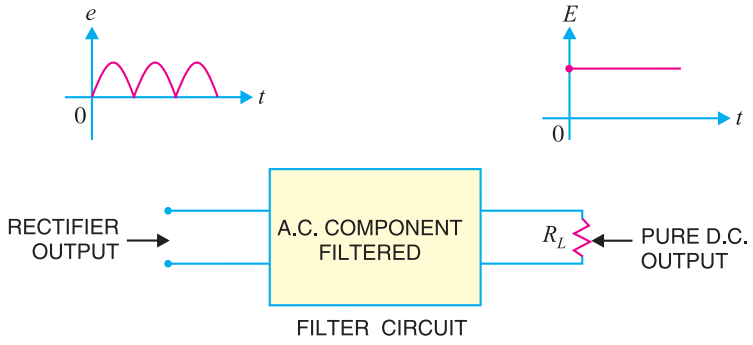


Fig. 6.40

6.21 Types of Filter Circuits

The most commonly used filter circuits are *capacitor filter*, *choke input filter* and *capacitor input filter or π-filter*. We shall discuss these filters in turn.

(*i*) Capacitor filter. Fig. 6.41 (*ii*) shows a typical capacitor filter circuit. It consists of a capacitor C placed across the rectifier output in parallel with load R_L. The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor and also supplies current to the load. At the end of quarter cycle [Point A in Fig. 6.41 (*iii*)], the

* If such a d.c. is applied in an electronic circuit, it will produce a *hum.*

** A capacitor offers infinite reactance to d.c. For d.c., $f = 0$.

$$\therefore \quad X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 0 \times C} = \infty$$

Hence, a capacitor does not allow d.c. to pass through it.

† We know $X_L = 2\pi fL$. For d.c., $f = 0$ and, therefore, $X_L = 0$. Hence inductor passes d.c. quite readily. For a.c., it offers opposition and drops a part of it.

capacitor is charged to the peak value V_m of the rectifier voltage. Now, the rectifier voltage starts to decrease. As this occurs, the capacitor discharges through the load and voltage across it (*i.e.* across parallel combination of *R-C*) decreases as shown by the line *AB* in Fig. 6.41 (*iii*). The voltage across load will decrease only slightly because immediately the next voltage peak comes and recharges the capacitor. This process is repeated again and again and the output voltage waveform becomes *ABCDEFG*. It may be seen that very little ripple is left in the output. Moreover, output voltage is higher as it remains substantially near the peak value of rectifier output voltage.

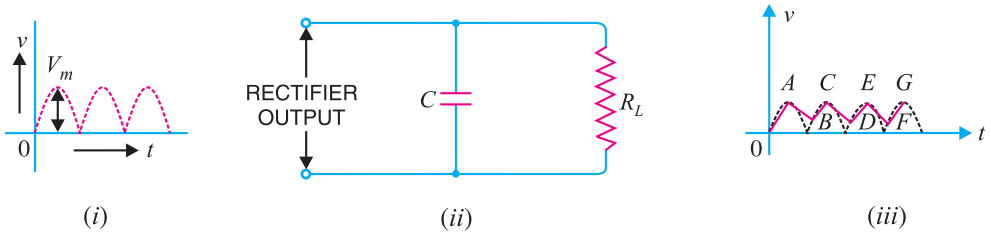


Fig. 6.41

The capacitor filter circuit is extremely popular because of its low cost, small size, little weight and good characteristics. For small load currents (say upto 50 mA), this type of filter is preferred. It is commonly used in transistor radio battery eliminators.

***(ii)* Choke input filter.** Fig. 6.42 shows a typical choke input filter circuit. It consists of a *choke *L* connected in series with the rectifier output and a filter capacitor *C* across the load. Only a single filter section is shown, but several identical sections are often used to reduce the pulsations as effectively as possible.

The pulsating output of the rectifier is applied across terminals 1 and 2 of the filter circuit. As discussed before, the pulsating output of rectifier contains a.c. and d.c. components. The choke offers high opposition to the passage of a.c. component but negligible opposition to the d.c. component. The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at terminal 3.

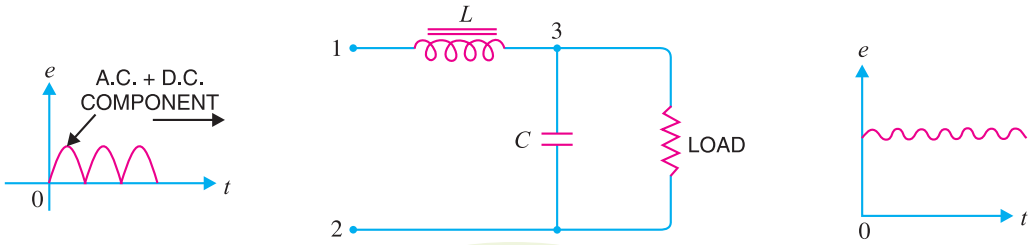


Fig. 6.42

At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which has managed to pass through the choke. Now, the low reactance of filter capacitor bypasses the a.c. component but prevents the d.c. component to flow through it. Therefore, only d.c. component reaches the load. In this way, the filter circuit has filtered out the a.c. component from the rectifier output, allowing d.c. component to reach the load.

***(iii)* Capacitor input filter *or* π-filter.** Fig. 6.43 shows a typical capacitor input filter or **π-filter. It consists of a filter capacitor C_1 connected across the rectifier output, a choke *L* in series and

* The shorthand name of inductor coil is choke.

** The shape of the circuit diagram of this filter circuit appears like Greek letter π (pi) and hence the name π-filter.

another filter capacitor C_2 connected across the load. Only one filter section is shown but several identical sections are often used to improve the smoothing action.

The pulsating output from the rectifier is applied across the input terminals (*i.e.* terminals 1 and 2) of the filter. The filtering action of the three components *viz* C_1, L and C_2 of this filter is described below :

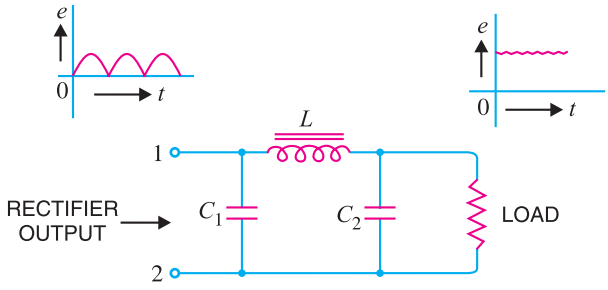


Fig. 6.43

(*a*) The *filter capacitor* C_1 offers low reactance to a.c. component of rectifier output while it offers infinite reactance to the d.c. component. Therefore, capacitor C_1 bypasses an appreciable amount of a.c. component while the d.c. component continues its journey to the choke L.

(*b*) The *choke* L offers high reactance to the a.c. component but it offers almost zero reactance to the d.c. component. Therefore, it allows the d.c. component to flow through it, while the *unbypassed a.c. component is blocked.

(*c*) The *filter capacitor* C_2 bypasses the a.c. component which the choke has failed to block. Therefore, only d.c. component appears across the load and that is what we desire.

Example 6.23. *For the circuit shown in Fig. 6.44, find the output d.c. voltage.*

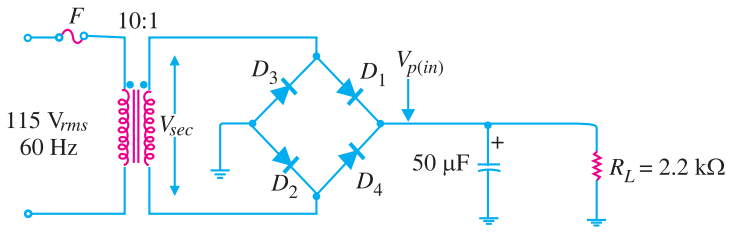


Fig. 6.44

Solution. It can be proved that output d.c. voltage is given by :

$$V_{dc} = V_{p(in)}\left(1 - \frac{1}{2f\ R_L C}\right)$$

Here $V_{p(in)}$ = Peak rectified full-wave voltage applied to the filter

f = Output frequency

Peak primary voltage, $V_{p(prim)} = \sqrt{2} \times 115 = 163\text{V}$

Peak secondary voltage, $V_{p(sec)} = \left(\frac{1}{10}\right) \times 163 = 16.3\text{V}$

Peak full-wave rectified voltage at the filter input is

$$V_{p\,(in)} = V_{p\,(sec)} - 2{\times}0.7 = 16.3 - 1.4 = 14.9\text{V}$$

For full-wave rectification, $f = 2\ f_{in} = 2{\times}60 = 120$ Hz

Now $$\frac{1}{2f\ R_L C} = \frac{1}{2 \times 120 \times (2.2{\times}10^3) \times (50 \times 10^{-6})} = 0.038$$

* That part of a.c. component which could not be bypassed by capacitor C_1.

$$\therefore \quad V_{dc} = V_{p(in)}\left(1 - \frac{1}{2f\,R_L C}\right) = 14.9\,(1 - 0.038) = \mathbf{14.3V}$$

Example 6.24. *The choke of Fig. 6.45 has a d.c. resistance of 25 Ω. What is the d.c. voltage if the full-wave signal into the choke has a peak value of 25.7 V ?*

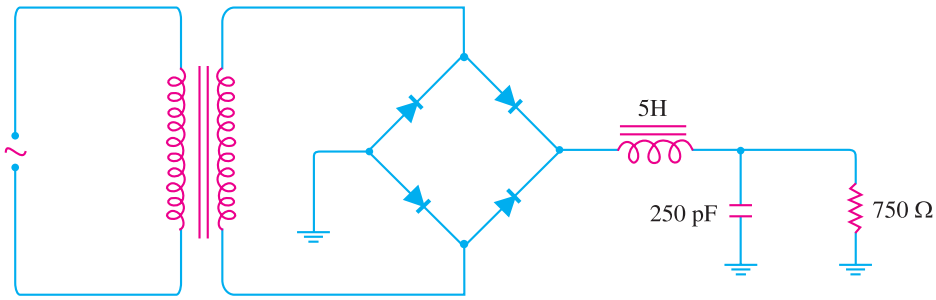


Fig. 6.45

Solution. The output of a full-wave rectifier has a d.c. component and an a.c. component. Due to the presence of a.c. component, the rectifier output has a pulsating character as shown in Fig. 6.46. The maximum value of the pulsating output is V_m and d.c. component is $V'_{dc} = 2\,V_m/\pi$.

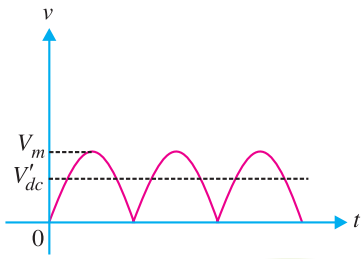


Fig. 6.46

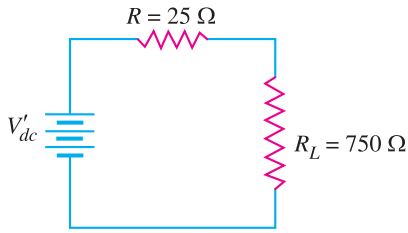


Fig. 6.47

For d.c. component V'_{dc}, the choke resistance is in series with the load as shown in Fig. 6.47.

$$\therefore \quad \text{Voltage across load, } V_{dc} = \frac{V'_{dc}}{R + R_L} \times R_L$$

$$\text{In our example, } V'_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 25.7}{\pi} = 16.4 \text{ V}$$

$$\therefore \quad \text{Voltage across load, } V_{dc} = \frac{V'_{dc}}{R + R_L} \times R_L = \frac{16.4}{25 + 750} \times 750 = \mathbf{15.9\ V}$$

The voltage across the load is 15.9 V dc *plus* a small ripple.

6.22 Voltage Multipliers

With a diode, we can build a rectifier to produce a d.c. voltage that is nearly equal to the peak value of input a.c. voltage. We can also use diodes and capacitors to build a circuit that will provide a *d.c output* that is multiple of the *peak input a.c. voltage.* Such a circuit is called a voltage multiplier. For example, a *voltage doubler* will provide a d.c. output that is *twice* the peak input a.c. voltage, a *voltage tripler* will provide a d.c. output that is three times the peak input a.c. voltage and so on.

While voltage multipliers provide d.c. output that is much greater than the peak input a.c. voltage, there is no power amplification and law of conservation of energy holds good. When a voltage multiplier *increases* the peak input voltage by a factor *n*, the peak input current is *decreased* by approximately the same factor. Thus the actual power output from a voltage multiplier will *never* be

greater than the input power. In fact, there are losses in the circuit (e.g. in diodes, capacitors etc.) so that the output power will actually be *less than* the input power.

6.23 Half-Wave Voltage Doubler

A half-wave voltage doubler consists of two diodes and two capacitors connected in a manner as shown in Fig. 6.48. It will be shown that if the peak input a.c. voltage is $V_{S(pk)}$, the d.c. output voltage will be 2 $V_{S(pk)}$ provided the diodes are ideal (this assumption is fairly reasonable). The basic idea in a voltage multiplier is to charge each capacitor to the peak input a.c. voltage and to arrange the capacitors so that their stored voltages will add.

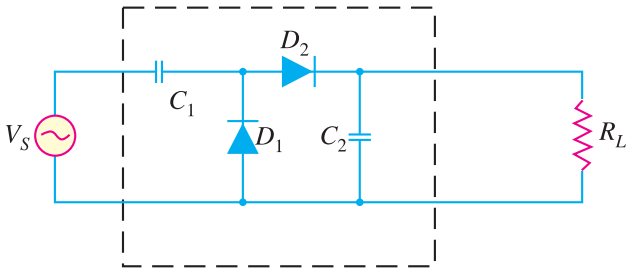


Fig. 6.48

Circuit action. We now discuss the working of a half-wave voltage doubler.

(i) During the negative half-cycle of a.c. input voltage [See Fig. 6.49 (*i*)], diode D_1 is forward biased and diode D_2 is reverse biased [See Fig. 6.49 (*i*)]. Therefore, diode D_1 can be represented by a *short* and diode D_2 as an *open*. The equivalent circuit then becomes as shown in Fig. 6.49 (*ii*).

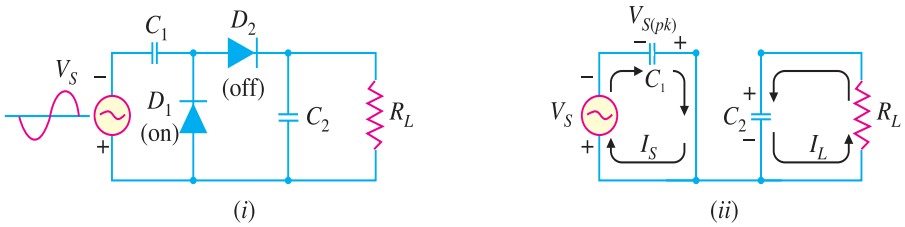


Fig. 6.49

As you can see [See Fig.6.49 (*ii*)], C_1 will charge until voltage across it becomes equal to peak value of source voltage [$V_{S(pk)}$]. At the same time, C_2 will be in the process of discharging through the load R_L (The source of this charge on C_2 will be explained in a moment). *Note that in all figures electron flow is shown.*

(ii) When the polarity of the input a.c. voltage reverses (*i.e.* during positive half-cycle), the circuit conditions become as shown in Fig. 6.50 (*i*). Now D_1 is reverse biased and D_2 is forward biased and the equivalent circuit becomes as shown in Fig. 6.50 (*ii*).

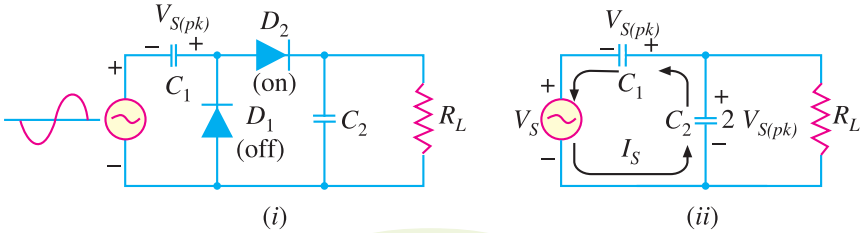


Fig. 6.50

Referring to Fig. 6.50 (*ii*), it is easy to see that C_1 (charged to $V_{S\,(pk)}$)and the source voltage (V_S) now act as *series-aiding* voltage sources. Thus C_2 will be charged to the sum of the series peak voltages *i.e.* $2\ V_{S(pk)}$.

(*iii*) When V_S returns to its original polarity (*i.e.* negative half-cycle), D_2 is again turned off (*i.e.* reverse biased). With D_2 turned off, the only discharge path for C_2 is through the load resistance R_L. The time constant ($= R_L\ C_2$) of this circuit is so adjusted that C_2 has little time to lose any of its charge before the input polarity reverses again. During the positive half-cycle, D_2 is turned on and C_2 recharges until voltage across it is again equal to $2\ V_{S\,(pk)}$.

$\therefore$ D.C. output voltage, $V_{dc} = 2\ V_{S\,(pk)}$

Since C_2 barely discharges between input cycles, the output waveform of the half-wave voltage doubler closely resembles that of a filtered half-wave rectifier. Fig. 6.51 shows the input and output waveforms for a half-wave voltage doubler.

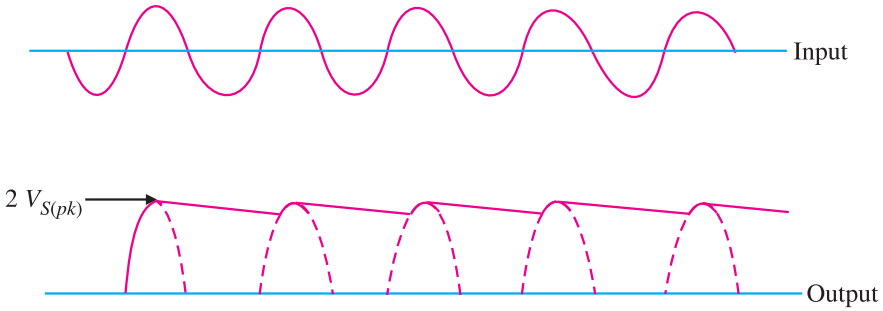


Fig. 6.51

The voltage multipliers have the disadvantage of poor voltage regulation. This means that d.c. output voltage drops considerably as the load current increases. Large filter capacitors are needed to help maintain the output voltage.

6.24 Voltage Stabilisation

A rectifier with an appropriate filter serves as a good source of d.c. output. However, the major disadvantage of such a power supply is that the output voltage changes with the variations in the input voltage or load. Thus, if the input voltage increases, the d.c. output voltage of the rectifier also increases. Similarly, if the load current increases, the output voltage falls due to the voltage drop in the rectifying element, filter chokes, transformer winding etc. In many electronic applications, it is desired that the output voltage should remain constant regardless of the variations in the input voltage or load. In order to ensure this, a voltage stabilising device, called voltage stabiliser is used. Several stabilising circuits have been designed but only *zener diode* as a voltage stabiliser will be discussed.

6.25 Zener Diode

It has already been discussed that when the reverse bias on a crystal diode is increased, a critical voltage, called *breakdown voltage* is reached where the reverse current increases sharply to a high value. The breakdown region is the knee of the reverse characteristic as shown in Fig. 6.52. The satisfactory explanation of this breakdown of the junction was first given by the American scientist *C.* Zener. Therefore, the breakdown voltage is sometimes called *zener voltage* and the sudden increase in current is known as zener current.

The breakdown or zener voltage depends upon the amount of doping. If the diode is heavily doped, depletion layer will be thin and consequently the breakdown of the junction will occur at a lower reverse voltage. On the other hand, a lightly doped diode has a higher breakdown voltage. When an ordinary crystal diode is properly doped so that it has a sharp breakdown voltage, it is called

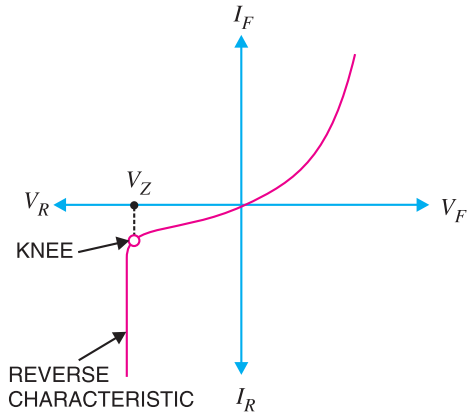


Fig. 6.52

a zener diode.

A properly doped crystal diode which has a sharp breakdown voltage is known as a **zener diode.**

Fig. 6.53 shows the symbol of a zener diode. It may be seen that it is just like an ordinary diode except that the bar is turned into z-shape. The following points may be noted about the zener diode:

(*i*) A zener diode is like an ordinary diode except that it is properly doped so as to have a sharp breakdown voltage.

(*ii*) A zener diode is always reverse connected *i.e.* it is always reverse biased.

(*iii*) A zener diode has sharp breakdown voltage, called zener voltage V_Z.

(*iv*) When forward biased, its characteristics are just those of ordinary diode.

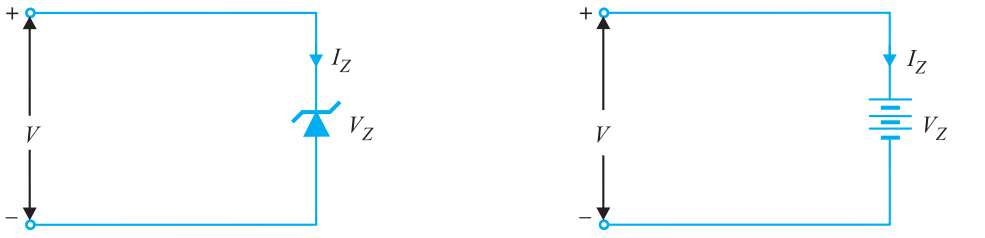
(*v*) The zener diode is not immediately burnt just because it has entered the *breakdown region. As long as the external circuit connected to the diode limits the diode current to less than *burn out* value, the diode will not burn out.

Fig. 6.53

6.26 Equivalent Circuit of Zener Diode

The analysis of circuits using zener diodes can be made quite easily by replacing the zener diode by its equivalent circuit.

(*i*) "On" state. When reverse voltage across a zener diode is equal to or more than break down voltage V_Z, the current increases very sharply. In this region, the curve is almost vertical. It means that voltage across zener diode is constant at V_Z even though the current through it changes. Therefore, in the breakdown region, an **ideal zener diode can be represented by a battery of voltage V_Z as shown in Fig. 6.54 (*ii*). Under such conditions, the zener diode is said to be in the "ON" state.



(*i*)
$V \geq V_Z$

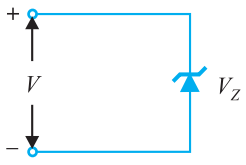
(*ii*)
Equivalent circuit of zener for ''on'' state

Fig. 6.54

(*ii*) "OFF" state. When the reverse voltage across the zener diode is less than V_Z but greater than 0 V, the zener diode is in the "OFF" state. Under such conditions, the zener diode can be represented by an open-circuit as shown in Fig. 6.55 (*ii*).

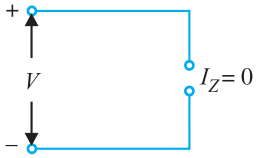
* The current is limited only by both external resistance and the power dissipation of zener diode.

** This assumption is fairly reasonable as the impedance of zener diode is quite small in the breakdown region.



(*i*)

$V_Z > V > 0$



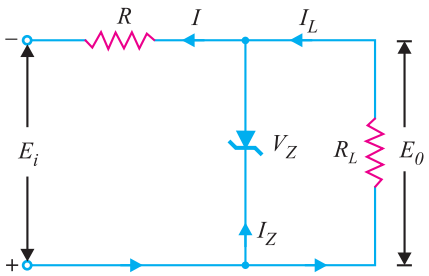
(*ii*)

Equivalent circuit of zener for ''off'' state

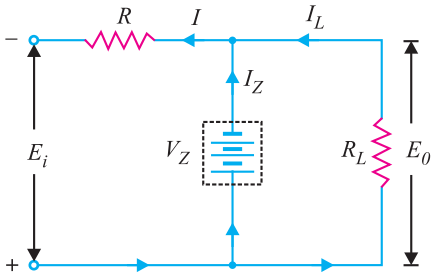
Fig. 6.55

6.27 Zener Diode as Voltage Stabiliser

A zener diode can be used as a voltage regulator to provide a constant voltage from a source whose voltage may vary over sufficient range. The circuit arrangement is shown in Fig. 6.56 (*i*). The zener diode of zener voltage V_Z is reverse connected across the load R_L across which constant output is desired. The series resistance R absorbs the output voltage fluctuations so as to maintain constant voltage across the load. It may be noted that the zener will maintain a constant voltage V_Z (= E_0) across the load so long as the input voltage does not fall below V_Z.



(*i*)



(*ii*)

Fig. 6.56

When the circuit is properly designed, the load voltage E_0 remains essentially constant (equal to V_Z) even though the input voltage E_i and load resistance R_L may vary over a wide range.

(i) Suppose the input voltage increases. Since the zener is in the breakdown region, the zener diode is equivalent to a battery V_Z as shown in Fig. 6.56 (*ii*). It is clear that output voltage remains constant at V_Z (= E_0). The excess voltage is dropped across the series resistance R. This will cause an increase in the value of total current I. The zener will conduct the increase of current in I while the load current remains constant. Hence, output voltage E_0 remains constant irrespective of the changes in the input voltage E_i.

(ii) Now suppose that input voltage is constant but the load resistance R_L decreases. This will cause an increase in load current. The extra current cannot come from the source because drop in R (and hence source current I) will not change as the zener is within its regulating range. The additional load current will come from a decrease in zener current I_Z. Consequently, the output voltage stays at constant value.

Voltage drop across $R = E_i - E_0$

Current through R, $I = I_Z + I_L$

Applying Ohm's law, we have,

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

6.28 Solving Zener Diode Circuits

The analysis of zener diode circuits is quite similar to that applied to the analysis of semiconductor diodes. The first step is to determine the state of zener diode *i.e.*, whether the zener is in the "on" state or "off" state. Next, the zener is replaced by its appropriate model. Finally, the unknown quantities are determined from the resulting circuit.

1. E_i and R_L fixed. This is the simplest case and is shown in Fig. 6.57 (*i*). Here the applied voltage E_i as well as load R_L is fixed. The first step is to find the state of zener diode. This can be determined by removing the zener from the circuit and calculating the voltage V across the resulting open-circuit as shown in Fig. 6.57 (*ii*).

$$V = E_0 = \frac{R_L E_i}{R + R_L}$$

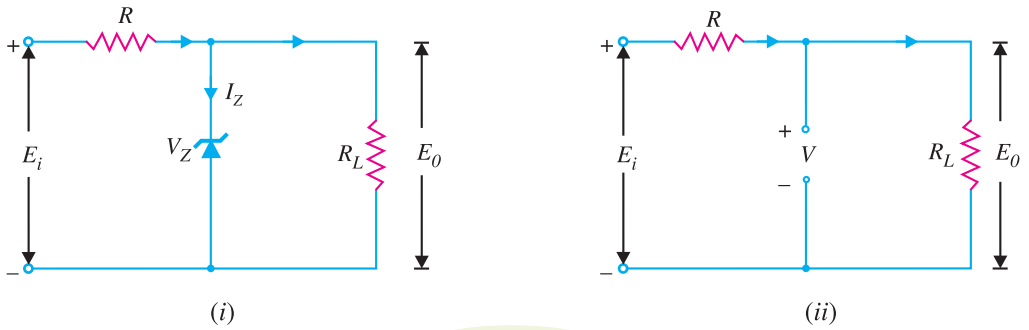


Fig. 6.57

If $V \geq V_Z$, the zener diode is in the "on" state and its equivalent model can be substituted as shown in Fig. 6.58 (*i*). If $V < V_Z$, the diode is in the "off" state as shown in Fig. 6.58 (*ii*).

***(i)* On state.** Referring to circuit shown in Fig. 6.58 (*i*),

$$E_0 = V_Z$$

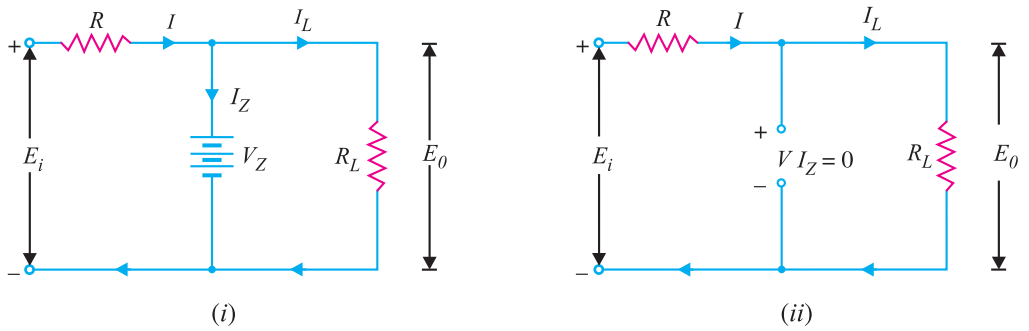


Fig. 6.58

$$I_Z = I - I_L \quad \text{where } I_L = \frac{E_0}{R_L} \text{ and } I = \frac{E_i - E_0}{R}$$

Power dissipated in zener, $P_Z = V_Z I_Z$

***(ii)* Off state.** Referring to the circuit shown in Fig. 6.58 (*ii*),

$$I = I_L \quad \text{and} \quad I_Z = 0$$
$$V_R = E_i - E_0 \quad \text{and} \quad V = E_0 \quad (V < V_Z)$$
$$\therefore \quad P_Z = V I_Z = V(0) = 0$$

2. Fixed E_i and Variable R_L. This case is shown in Fig. 6.59. Here the applied voltage (E_i) is fixed while load resistance R_L (and hence load current I_L) changes. Note that there is a definite range of R_L values (and hence I_L values) which will ensure the zener diode to be in "on" state. Let us calculate that range of values.

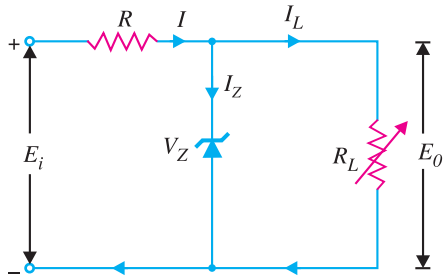


Fig. 6.59

***(i)* R_{Lmin} and I_{Lmax}.** Once the zener is in the "on" state, load voltage E_0 (= V_Z) is constant. As a result, when load resistance is minimum (*i.e.*, R_{Lmin}), load current will be maximum ($I_L = E_0/R_L$). In order to find the minimum load resistance that will turn the zener on, we simply calculate the value of R_L that will result in $E_0 = V_Z$ *i.e.*,

$$E_0 = V_Z = {}^{*}\frac{R_L E_i}{R + R_L}$$

$$\therefore \quad R_{Lmin} = \frac{R V_Z}{E_i - V_Z} \qquad \ldots(i)$$

This is the minimum value of load resistance that will ensure that zener is in the "on" state. Any value of load resistance less than this value will result in a voltage E_0 across the load less than V_Z and the zener will be in the "off" state.

Clearly ; $$I_{Lmax} = \frac{E_0}{R_{Lmin}} = \frac{V_Z}{R_{Lmin}}$$

***(ii)* I_{Lmin} and R_{Lmax}.** It is easy to see that when load resistance is maximum, load current is minimum.

Now, Zener current, $I_Z = I - I_L$

When the zener is in the "on" state, I remains **fixed. This means that when I_L is maximum, I_Z will be minimum. On the other hand, when I_L is minimum, I_Z is maximum. If the maximum current that a zener can carry safely is †I_{ZM}, then,

---

* If you remove the zener in the circuit shown in Fig. 6.59, then voltage V across the open-circuit is

$$V = \frac{R_L E_i}{R + R_L}$$

The zener will be turned on when $V = V_Z$.

** Voltage across R, $V_R = E_i - E_0$ and $I = V_R/R$. As E_i and E_0 are fixed, I remains the same.

† Max. power dissipation in zener, $P_{ZM} = V_Z I_{ZM}$

$$I_{Lmin} = I - I_{ZM}$$

and $$R_{Lmax} = \frac{E_0}{I_{Lmin}} = \frac{V_Z}{I_{Lmin}}$$

If the load resistance exceeds this limiting value, the current through zener will exceed I_{ZM} and the device may burn out.

3. Fixed R_L and Variable E_i. This case is shown in Fig. 6.60. Here the load resistance R_L is fixed while the applied voltage (E_i) changes. Note that there is a definite range of E_i values that will ensure that zener diode is in the "on" state. Let us calculate that range of values.

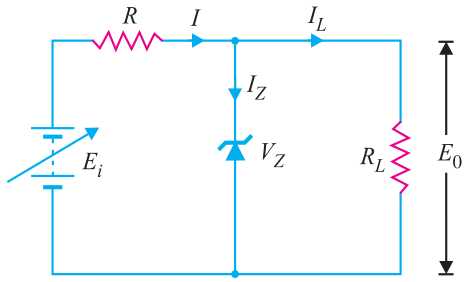


Fig. 6.60

(i) E_i (min). To determine the minimum applied voltage that will turn the zener on, simply calculate the value of E_i that will result in load voltage $E_0 = V_Z$ *i.e.*,

$$E_0 = V_Z = \frac{R_L E_i}{R + R_L}$$

$$\therefore \quad E_{i\,(min)} = \frac{(R + R_L) V_Z}{R_L}$$

(ii) E_i (max)

Now, current through R, $I = I_Z + I_L$

Since I_L ($= E_0/R_L = V_Z/R_L$) is fixed, the value of I will be maximum when zener current is maximum *i.e.*,

$$I_{max} = I_{ZM} + I_L$$

Now $$E_i = I R + E_0$$

Since E_0 ($= V_Z$) is constant, the input voltage will be maximum when I is maximum.

$$\therefore \quad E_{i\,(max)} = I_{max} R + V_Z$$

Example 6.25. *For the circuit shown in Fig. 6.61 (i), find :*

(i) the output voltage *(ii) the voltage drop across series resistance*

(iii) the current through zener diode.

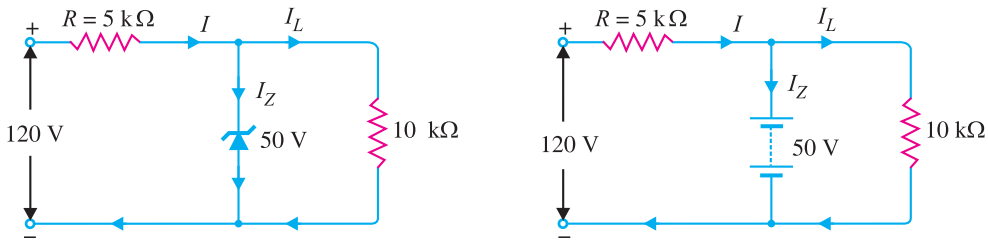


Fig. 6.61

Solution. If you remove the zener diode in Fig. 6.61 (*i*), the voltage V across the open-circuit is given by :

$$V = \frac{R_L E_i}{R + R_L} = \frac{10 \times 120}{5 + 10} = 80 \text{ V}$$

Since voltage across zener diode is greater than V_Z (= 50 V), the zener is in the "on" state. It can, therefore, be represented by a battery of 50 V as shown in Fig. 6.61 (*ii*).

(*i*) Referring to Fig. 6.61 (*ii*),

Output voltage $= V_Z =$ **50 V**

(*ii*) Voltage drop across R = Input voltage $- V_Z = 120 - 50 =$ **70 V**

(*iii*) Load current, $I_L = V_Z/R_L = 50 \text{ V}/10 \text{ k}\Omega = 5 \text{ mA}$

Current through R, $I = \frac{70 \text{ V}}{5 \text{ k}\Omega} = 14 \text{ mA}$

Applying Kirchhoff's first law, $I = I_L + I_Z$

$\therefore$ Zener current, $I_Z = I - I_L = 14 - 5 =$ **9 mA**

Example 6.26. *For the circuit shown in Fig. 6.62 (i), find the maximum and minimum values of zener diode current.*

Solution. The first step is to determine the state of the zener diode. It is easy to see that for the given range of voltages (80 – 120 V), the voltage across the zener is greater than V_Z (= 50 V). Hence the zener diode will be in the "on" state for this range of applied voltages. Consequently, it can be replaced by a battery of 50 V as shown in Fig. 6.62 (*ii*).

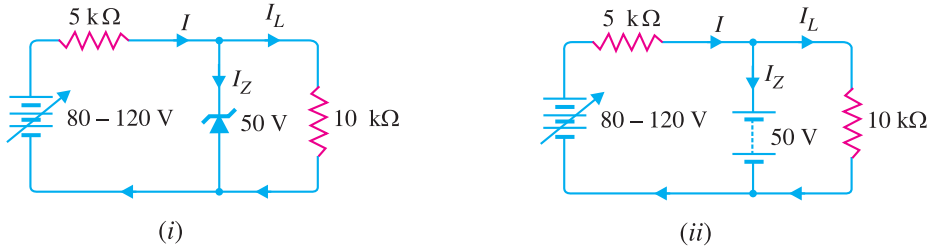


Fig. 6.62

Maximum zener current. The zener will conduct *maximum current when the input voltage is maximum *i.e.* 120 V. Under such conditions :

Voltage across 5 kΩ = 120 – 50 = 70 V

Current through 5 kΩ, $I = \frac{70 \text{ V}}{5 \text{ k}\Omega} = 14 \text{ mA}$

Load current, $I_L = \frac{50 \text{ V}}{10 \text{ k}\Omega} = 5 \text{ mA}$

Applying Kirchhoff's first law, $I = I_L + I_Z$

$\therefore$ Zener current, $I_Z = I - I_L = 14 - 5 =$ **9 mA**

* $I_Z = I - I_L$. Since I_L ($= V_Z/R_L$) is fixed, I_Z will be maximum when I is maximum.

Now, $I = \frac{E_i - E_0}{R} = \frac{E_i - V_Z}{R}$. Since V_Z ($= E_0$) and R are fixed, I will be maximum when E_i is maximum and *vice-versa*.

Minimum Zener current. The zener will conduct minimum current when the input voltage is minimum *i.e.* 80 V. Under such conditions, we have,

Voltage across 5 kΩ = 80 – 50 = 30 V

Current through 5 kΩ, $I = \frac{30\text{ V}}{5\text{ k}\Omega} = 6\text{ mA}$

Load current, $I_L = 5\text{ mA}$

$\therefore$ Zener current, $I_Z = I - I_L = 6 - 5 = \mathbf{1\text{ mA}}$

Example 6.27. *A 7.2 V zener is used in the circuit shown in Fig. 6.63 and the load current is to vary from 12 to 100 mA. Find the value of series resistance R to maintain a voltage of 7.2 V across the load. The input voltage is constant at 12V and the minimum zener current is 10 mA.*

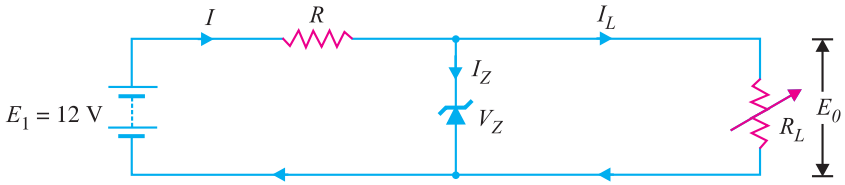


Fig. 6.63

Solution. $E_i = 12\text{ V}$; $V_Z = 7.2\text{ V}$

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

The voltage across R is to remain constant at 12 – 7.2 = 4.8 V as the load current changes from 12 to 100 mA. The minimum zener current will occur when the load current is maximum.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{12\text{ V} - 7.2\text{ V}}{(10 + 100)\text{ mA}} = \frac{4.8\text{ V}}{110\text{ mA}} = \mathbf{43.5\ \Omega}$$

If $R = 43.5\ \Omega$ is inserted in the circuit, the output voltage will remain constant over the regulating range. As the load current I_L decreases, the zener current I_Z will increase to such a value that $I_Z + I_L =$ 110 mA. Note that if load resistance is open-circuited, then $I_L = 0$ and zener current becomes 110 mA.

Example 6.28. *The zener diode shown in Fig. 6.64 has $V_Z = 18$ V. The voltage across the load stays at 18 V as long as I_Z is maintained between 200 mA and 2 A. Find the value of series resistance R so that E_0 remains 18 V while input voltage E_i is free to vary between 22 V to 28V.*

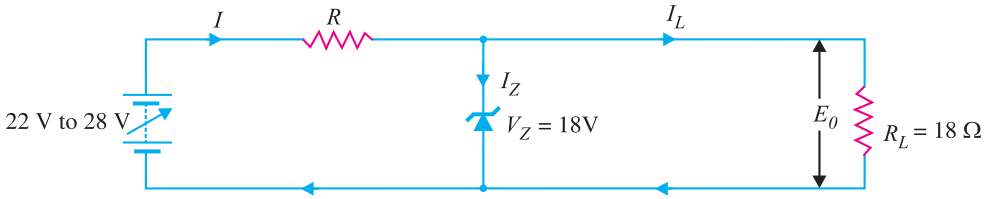


Fig. 6.64

Solution. The zener current will be minimum (*i.e.* 200 mA) when the input voltage is minimum (*i.e.* 22 V). The load current stays at constant value $I_L = V_Z / R_L = 18\text{ V}/18\ \Omega = 1\text{ A} = 1000\text{ mA}$.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{(22 - 18)\text{ V}}{(200 + 1000)\text{ mA}} = \frac{4\text{ V}}{1200\text{ mA}} = \mathbf{3.33\ \Omega}$$

Example 6.29. *A 10-V zener diode is used to regulate the voltage across a variable load resistor [See fig. 6.65]. The input voltage varies between 13 V and 16 V and the load current varies between 10 mA and 85 mA. The minimum zener current is 15 mA. Calculate the value of series resistance R.*

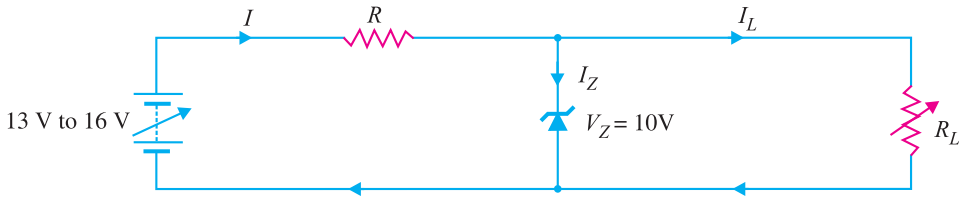


Fig. 6.65

Solution. The zener will conduct minimum current (*i.e.* 15 mA) when input voltage is minimum (*i.e.* 13 V).

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{(13 - 10)\text{ V}}{(15 + 85)\text{ mA}} = \frac{3\text{ V}}{100\text{ mA}} = \mathbf{30\ \Omega}$$

Example 6.30. *The circuit of Fig. 6.66 uses two zener diodes, each rated at 15 V, 200 mA. If the circuit is connected to a 45-volt unregulated supply, determine :*

(i) The regulated output voltage *(ii) The value of series resistance R*

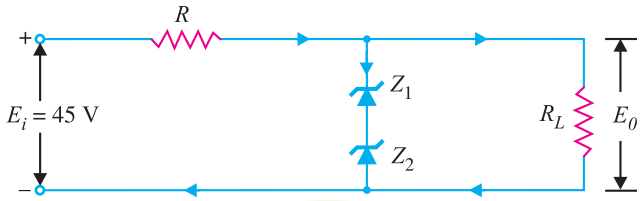


Fig. 6.66

Solution. When the desired regulated output voltage is higher than the rated voltage of the zener, two or more zeners are connected in series as shown in Fig. 6.66. However, in such circuits, care must be taken to select those zeners that have the same current rating.

Current rating of each zener, I_Z = 200 mA

Voltage rating of each zener, V_Z = 15 V

Input voltage, E_i = 45 V

(i) Regulated output voltage, E_0 = 15 + 15 = **30 V**

(ii) Series resistance, $R = \dfrac{E_i - E_0}{I_Z} = \dfrac{45 - 30}{200\text{ mA}} = \dfrac{15\text{ V}}{200\text{ mA}} = \mathbf{75\ \Omega}$

Example 6.31. *What value of series resistance is required when three 10-watt, 10-volt, 1000 mA zener diodes are connected in series to obtain a 30-volt regulated output from a 45 volt d.c. power source ?*

Solution. Fig. 6.67 shows the desired circuit. The worst case is at no load because then zeners carry the maximum current.

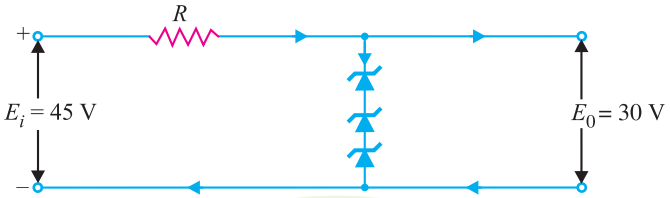


Fig. 6.67

Voltage rating of each zener, $V_Z = 10\,V$

Current rating of each zener, $I_Z = 1000\,mA$

Input unregulated voltage, $E_i = 45\,V$

Regulated output voltage, $E_0 = 10 + 10 + 10 = 30\,V$

Let R ohms be the required series resistance.

Voltage across $R = E_i - E_0 = 45 - 30 = 15\,V$

$$\therefore \quad R = \frac{E_i - E_0}{I_Z} = \frac{15\,V}{1000\,mA} = \mathbf{15\,\Omega}$$

Example 6.32. *Over what range of input voltage will the zener circuit shown in Fig. 6.68 maintain 30 V across 2000 Ω load, assuming that series resistance R = 200 Ω and zener current rating is 25 mA ?*

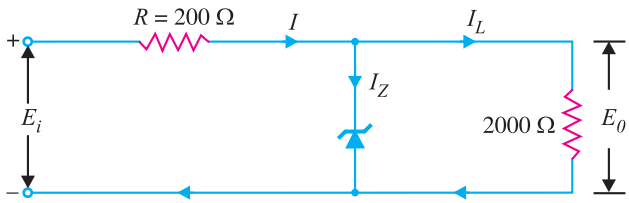


Fig. 6.68

Solution. The minimum input voltage required will be when $I_Z = 0$. Under this condition,

$$I_L = I = \frac{30\,V}{2000\,\Omega} = 15\,mA$$

$$\therefore \quad \text{Minimum input voltage} = 30 + I\,R = 30 + 15\,mA \times 200\,\Omega$$
$$= 30 + 3 = \mathbf{33\,V}$$

The maximum input voltage required will be when $I_Z = 25$ mA. Under this condition,

$$I = I_L + I_Z = 15 + 25 = 40\,mA$$

$$\therefore \quad \text{Max. input voltage} = 30 + I\,R$$
$$= 30 + 40\,mA \times 200\,\Omega$$
$$= 30 + 8 = \mathbf{38\,V}$$

Therefore, the input voltage range over which the circuit will maintain 30 V across the load is **33 V to 38 V.**

Example 6.33. *In the circuit shown in Fig. 6.69, the voltage across the load is to be maintained at 12 V as load current varies from 0 to 200 mA. Design the regulator. Also find the maximum wattage rating of zener diode.*

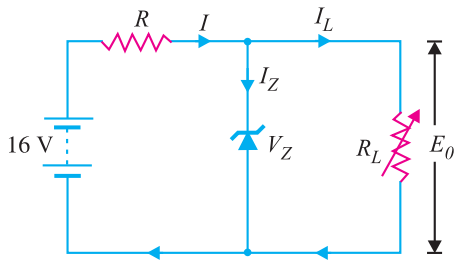


Fig. 6.69

Solution. By designing the regulator here means to find the values of V_Z and R. Since the load voltage is to be maintained at 12 V, we will use a zener diode of zener voltage 12 V *i.e.*,

$$V_Z = \mathbf{12\,V}$$

The voltage across R is to remain constant at $16 - 12 = 4$ V as the load current changes from 0 to 200 mA. The minimum zener current will occur when the load current is maximum.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{16 - 12}{(0 + 200)\,mA} = \frac{4\,V}{200\,mA} = \mathbf{20\,\Omega}$$

Maximum power rating of zener is

$$P_{ZM} = V_Z I_{ZM} = (12 \text{ V})(200 \text{ mA}) = \mathbf{2.4\ W}$$

Example. 6.34. *Fig. 6.70 shows the basic zener diode circuits. What will be the circuit behaviour if the zener is (i) working properly (ii) shorted (iii) open-circuited?*

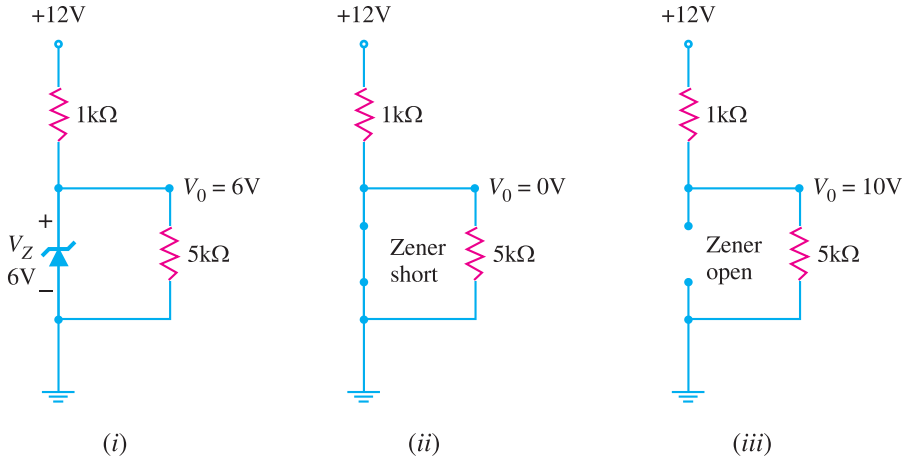


Fig. 6.70

Solution. Zener diodes cannot be tested individually with a multimeter. It is because multimeters usually do not have enough input voltage to put the zener into breakdown region.

(*i*) If the zener diode is working properly, the voltage V_0 across the load (= 5 kΩ) will be nearly 6V [See Fig. 6.70 (*i*)].

(*ii*) If the zener diode is short [See Fig. 6.70 (*ii*)], you will measure V_0 as 0V. The same problem could also be caused by a shorted load resistor (= 5kΩ) or an opened source resistor (= 1 kΩ). The only way to tell which device has failed is to remove the resistors and check them with an ohmmeter. If the resistors are good, then zener diode is bad.

(*iii*) If the zener diode is open-circuited, the voltage V_0 across the load (= 5 kΩ) will be 10V.

Example 6.35. *Fig. 6.71 shows regulated power supply using a zener diode. What will be the circuit behaviour if (i) filter capacitor shorts (ii) filter capacitor opens?*

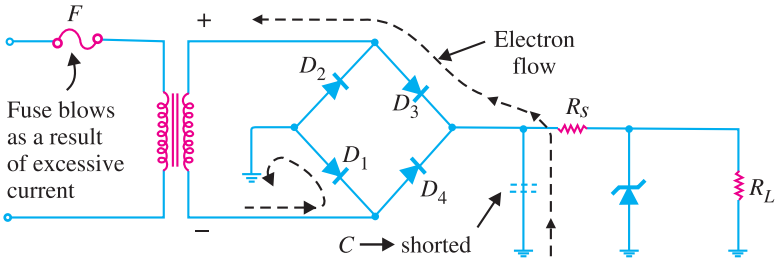


Fig. 6.71

Solution. The common faults in a zener voltage regulator are shorted filter capacitor or opened filter capacitor.

(*i*) When filter capacitor shorts. When the filter capacitor shorts, the primary fuse will blow. The reason for this is illustrated in Fig. 6.71. When the filter capacitor shorts, it shorts out the load resistance R_L. This has the same effect as wiring the two sides of the bridge together (See Fig. 6.71).

If you trace from the high side of the bridge to the low side, you will see that the only resistance across the secondary of the transformer is the forward resistance of the two *ON* diodes. This effectively shorts out the transformer secondary. The result is that excessive current flows in the secondary and hence in the primary. Consequently, the primary fuse will blow.

(*ii*) When filter capacitor opens. When the filter capacitor opens, it will cause the ripple in the power supply output to increase drastically. At the same time, the d.c. output voltage will show a significant drop. Since an open filter capacitor is the only fault that will cause *both* of these symptoms, no further testing is necessary. If both symptoms appear, replace the filter capacitor.

6.29 Crystal Diodes versus Vacuum Diodes

Semiconductor diodes (or crystal diodes) have a number of advantages and disadvantages as compared to their electron-tube counterparts (*i.e.*, vacuum diodes).

Advantages :

(*i*) They are smaller, more rugged and have a longer life.

(*ii*) They are simpler and inherently cheaper.

(*iii*) They require no filament power. As a result, they produce less heat than the equivalent vacuum diodes.

Disadvantages :

(*i*) They are extremely heat sensitive. Even a slight rise in temperature increases the current appreciably. Should the temperature *exceed the rated value of the diode, the increased flow of current may produce enough heat to ruin the *pn* junction. On the other hand, vacuum diodes function normally over a wide range of temperature changes.

It may be noted that silicon is better than germanium as a semiconductor material. Whereas a germanium diode should not be operated at temperatures higher than 80ºC, silicon diodes may operate safely at temperatures upto about 200ºC.

(*ii*) They can handle small currents and low inverse voltages as compared to vacuum diodes.

(*iii*) They cannot stand an overload even for a short period. Any slight overload, even a transient pulse, may permanently damage the crystal diode. On the other hand, vacuum diodes can stand an overload for a short period and when the overload is removed, the tube will generally recover.

MULTIPLE-CHOICE QUESTIONS

1. A crystal diode has .....
- (*i*) one *pn* junction
- (*ii*) two *pn* junctions
- (*iii*) three *pn* junctions
- (*iv*) none of the above

2. A crystal diode has forward resistance of the order of .....
- (*i*) kΩ (*ii*) Ω
- (*iii*) MΩ (*iv*) none of the above

3. If the arrow of crystal diode symbol is positive w.r.t. bar, then diode is ..... biased.
- (*i*) forward
- (*ii*) reverse
- (*iii*) either forward or reverse
- (*iv*) none of the above

4. The reverse current in a diode is of the order of .....
- (*i*) kA (*ii*) mA
- (*iii*) μA (*iv*) A

5. The forward voltage drop across a silicon diode is about .....

* Even when soldering the leads of a crystal diode, care must be taken not to permit heat from the soldering device to reach the crystal diode.

(*i*) 2.5 V (*ii*) 3 V
(*iii*) 10 V (*iv*) 0.7 V

6. A crystal diode is used as .....
(*i*) an amplifier (*ii*) a rectifier
(*iii*) an oscillator (*iv*) a voltage regulator

7. The d.c. resistance of a crystal diode is ..... its a.c. resistance.
(*i*) the same as (*ii*) more than
(*iii*) less than (*iv*) none of the above

8. An ideal crystal diode is one which behaves as a perfect ..... when forward biased.
(*i*) conductor
(*ii*) insulator
(*iii*) resistance material
(*iv*) none of the above

9. The ratio of reverse resistance and forward resistance of a germanium crystal diode is about .....
(*i*) 1 : 1 (*ii*) 100 : 1
(*iii*) 1000 : 1 (*iv*) 40000 : 1

10. The leakage current in a crystal diode is due to .....
(*i*) minority carriers
(*ii*) majority carriers
(*iii*) junction capacitance
(*iv*) none of the above

11. If the temperature of a crystal diode increases, then leakage current .....
(*i*) remains the same
(*ii*) decreases
(*iii*) increases
(*iv*) becomes zero

12. The PIV rating of a crystal diode is ..... that of equivalent vacuum diode.
(*i*) the same as (*ii*) lower than
(*iii*) more than (*iv*) none of the above

13. If the doping level of a crystal diode is increased, the breakdown voltage .....
(*i*) remains the same
(*ii*) is increased
(*iii*) is decreased
(*iv*) none of the above

14. The knee voltage of a crystal diode is approximately equal to .....
(*i*) applied voltage
(*ii*) breakdown voltage
(*iii*) forward voltage
(*iv*) barrier potential

15. When the graph between current through and voltage across a device is a straight line, the device is referred to as .....
(*i*) linear (*ii*) active
(*iii*) nonlinear (*iv*) passive

16. When the crystal diode current is large, the bias is .....
(*i*) forward (*ii*) inverse
(*iii*) poor (*iv*) reverse

17. A crystal diode is a ..... device.
(*i*) non-linear (*ii*) bilateral
(*iii*) linear (*iv*) none of the above

18. A crystal diode utilises ..... characteristic for rectification.
(*i*) reverse (*ii*) forward
(*iii*) forward or reverse
(*iv*) none of the above

19. When a crystal diode is used as a rectifier, the most important consideration is .....
(*i*) forward characteristic
(*ii*) doping level
(*iii*) reverse characteristic
(*iv*) PIV rating

20. If the doping level in a crystal diode is increased, the width of depletion layer .....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

21. A zener diode has .....
(*i*) one *pn* junction
(*ii*) two *pn* junctions
(*iii*) three *pn* junctions
(*iv*) none of the above

22. A zener diode is used as .....
(*i*) an amplifier (*ii*) a voltage regulator
(*iii*) a rectifier (*iv*) a multivibrator

23. The doping level in a zener diode is ..... that of a crystal diode.

(*i*) the same as (*ii*) less than
(*iii*) more than (*iv*) none of the above

24. A zener diode is always ..... connected.
(*i*) reverse
(*ii*) forward
(*iii*) either reverse or forward
(*iv*) none of the above

25. A zener diode utilises ..... characteristic for its operation.
(*i*) forward
(*ii*) reverse
(*iii*) both forward and reverse
(*iv*) none of the above

26. In the breakdown region, a zener diode behaves like a ..... source.
(*i*) constant voltage
(*ii*) constant current
(*iii*) constant resistance
(*iv*) none of the above

27. A zener diode is destroyed if it .....
(*i*) is forward biased
(*ii*) is reverse biased
(*iii*) carries more than rated current
(*iv*) none of the above

28. A series resistance is connected in the zener circuit to .....
(*i*) properly reverse bias the zener
(*ii*) protect the zener
(*iii*) properly forward bias the zener
(*iv*) none of the above

29. A zener diode is ..... device.
(*i*) a non-linear (*ii*) a linear
(*iii*) an amplifying (*iv*) none of the above

30. A zener diode has ..... breakdown voltage.
(*i*) undefined (*ii*) sharp
(*iii*) zero (*iv*) none of the above

31. ..... rectifier has the lowest forward resistance.
(*i*) solid state (*ii*) vacuum tube
(*iii*) gas tube (*iv*) none of the above

32. Mains a.c. power is converted into d.c. power for .....
(*i*) lighting purposes
(*ii*) heaters
(*iii*) using in electronic equipment
(*iv*) none of the above

33. The disadvantage of a half-wave rectifier is that the .....
(*i*) components are expensive
(*ii*) diodes must have a higher power rating
(*iii*) output is difficult to filter
(*iv*) none of the above

34. If the a.c. input to a half-wave rectifier has an r.m.s. value of $400/\sqrt{2}$ volts, then diode PIV rating is .....
(*i*) $400/\sqrt{2}$ V (*ii*) 400 V
(*iii*) $400 \times \sqrt{2}$ V (*iv*) none of the above

35. The ripple factor of a half-wave rectifier is .....
(*i*) 2 (*ii*) 1.21
(*iii*) 2.5 (*iv*) 0.48

36. There is a need of transformer for .....
(*i*) half-wave rectifier
(*ii*) centre-tap full-wave rectifier
(*iii*) bridge full-wave rectifier
(*iv*) none of the above

37. The *PIV* rating of each diode in a bridge rectifier is ..... that of the equivalent centre-tap rectifier.
(*i*) one-half (*ii*) the same as
(*iii*) twice (*iv*) four times

38. For the same secondary voltage, the output voltage from a centre-tap rectifier is ..... than that of bridge rectifier.
(*i*) twice (*ii*) thrice
(*iii*) four times (*iv*) one-half

39. If the PIV rating of a diode is exceeded, ...
(*i*) the diode conducts poorly
(*ii*) the diode is destroyed
(*iii*) the diode behaves as zener diode
(*iv*) none of the above

40. A 10 V power supply would use ..... as filter capacitor.
(*i*) paper capacitor (*ii*) mica capacitor
(*iii*) electrolytic capacitor
(*iv*) air capacitor

41. A 1000 V power supply would use ..... as a filter capacitor.
(*i*) paper capacitor
(*ii*) air capacitor
(*iii*) mica capacitor
(*iv*) electrolytic capacitor

42. The ..... filter circuit results in the best voltage regulation.
(*i*) choke input
(*ii*) capacitor input
(*iii*) resistance input
(*iv*) none of the above

43. A half-wave rectifier has an input voltage of 240 V r.m.s. If the step-down transformer has a turns ratio of 8 : 1, what is the peak load voltage ? Ignore diode drop.
(*i*) 27.5 V (*ii*) 86.5 V
(*iii*) 30 V (*iv*) 42.5 V

44. The maximum efficiency of a half-wave rectifier is .....
(*i*) 40.6% (*ii*) 81.2%
(*iii*) 50% (*iv*) 25%

45. The most widely used rectifier is .....
(*i*) half-wave rectifier
(*ii*) centre-tap full-wave rectifier
(*iii*) bridge full-wave rectifier
(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*iii*)	**5.** (*iv*)
6. (*ii*)	**7.** (*iii*)	**8.** (*i*)	**9.** (*iv*)	**10.** (*i*)
11. (*iii*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*iv*)	**15.** (*i*)
16. (*i*)	**17.** (*i*)	**18.** (*ii*)	**19.** (*iv*)	**20.** (*iii*)
21. (*i*)	**22.** (*ii*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*i*)	**27.** (*iii*)	**28.** (*ii*)	**29.** (*i*)	**30.** (*ii*)
31. (*i*)	**32.** (*iii*)	**33.** (*iii*)	**34.** (*ii*)	**35.** (*iv*)
36. (*ii*)	**37.** (*i*)	**38.** (*iv*)	**39.** (*ii*)	**40.** (*iii*)
41. (*i*)	**42.** (*i*)	**43.** (*iv*)	**44.** (*i*)	**45.** (*iii*)

Chapter Review Topics

1. What is a crystal diode ? Explain its rectifying action.
2. Draw the graphic symbol of crystal diode and explain its significance. How the polarities of crystal diode are identified ?
3. What do you understand by the d.c. and a.c. resistance of a crystal diode ? How will you determine them from the *V-I* characteristic of a crystal diode ?
4. Draw the equivalent circuit of a crystal diode.
5. Discuss the importance of peak inverse voltage in rectifier service.
6. Describe a half-wave rectifier using a crystal diode.
7. Derive an expression for the efficiency of a half-wave rectifier.
8. With a neat sketch, explain the working of (*i*) Centre-tap full-wave rectifier (*ii*) Full-wave bridge rectifier.
9. Derive an expression for the efficiency for a full-wave rectifier.
10. Write a short note about the nature of rectifier output.
11. What is a ripple factor ? What is its value for a half-wave and full-wave rectifier ?
12. Describe the action of the following filter circuits : (*i*) capacitor filter (*ii*) choke input filter (*iii*) capacitor input filter.
13. What is a zener diode ? Draw the equivalent circuit of an ideal zener in the breakdown region.
14. Explain how zener diode maintains constant voltage across the load.

Problems

1. What is the current in the circuit in Fig. 6.72 ? Assume the diode to be ideal. **[10 mA]**

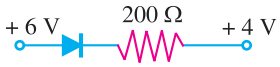


Fig. 6.72

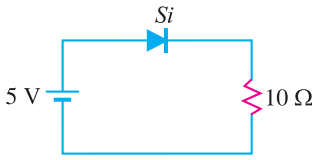


Fig. 6.73

2. Using equivalent circuit, determine the current in the circuit shown in Fig. 6.73. Assume the forward resistance of the diode to be 2 Ω. **[358 mA]**

3. Find the voltage V_A and current I in the circuit shown in Fig. 6.74. Use simplified model. **[14 V; 2 mA]**

4. Determine the magnitude of V_A in the circuit shown in Fig. 6.75. **[9.5 V]**

5. A half-wave rectifier uses a transformer of turn ratio 4 : 1. If the primary voltage is 240 V (r.m.s.), find (*i*) d.c. output voltage (*ii*) peak inverse voltage. Assume the diode to be ideal. **[(*i*) 27 V (*ii*) 85 V]**

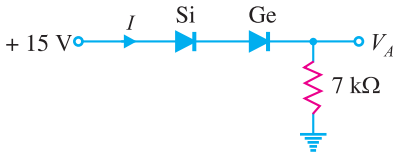


Fig. 6.74

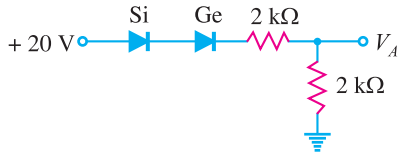


Fig. 6.75

6. A half-wave rectifier uses a transformer of turn ratio 2 : 1. The load resistance is 500 Ω. If the primary voltage (r.m.s.) is 240 V, find (*i*) d.c. output voltage (*ii*) peak inverse voltage. **[(*i*) 54 V (*ii*) 170 V]**

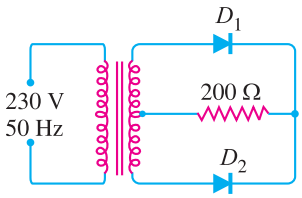


Fig. 6.76

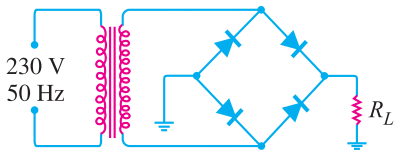


Fig. 6.77

7. In Fig. 6.76, the maximum voltage across half of secondary winding is 50 V. Find (*i*) the average load voltage (*ii*) peak inverse voltage (*iii*) output frequency. Assume the diodes to be ideal.

[(*i*) 31.8 V (*ii*) 100 V (*iii*) 100 Hz]

8. In Fig. 6.77, the maximum secondary voltage is 136 V. Find (*i*) the d.c. load voltage (*ii*) peak inverse voltage (*iii*) output frequency. **[(*i*) 86.6 V (*ii*) 136 V (*iii*) 100 Hz]**

9. A semiconductor diode having ideal forward and reverse characteristics is used in a half-wave rectifier circuit supplying a resistive load of 1000 Ω. If the r.m.s. value of the sinusoidal supply voltage is 250 V, determine (*i*) the r.m.s. diode current and (*ii*) power dissipated in the load.

[(*i*) 177 mA (*ii*) 31.3W]

10. The four semiconductor diodes used in a bridge rectifier circuit have forward resistance which can be considered constant at 0.1Ω and infinite reverse resistance. They supply a mean current of 10 A to a resistive load from a sinusoidally varying alternating supply of 20V r.m.s. Determine the resistance of the load and the efficiency of the circuit. **[1.6Ω ; 72%]**

11. Find the average value of each voltage in Fig. 6.78.

[(*i*) 1.59 V (*ii*) 63.7 V (*iii*) 16.4 V (*iv*) 10.5 V]

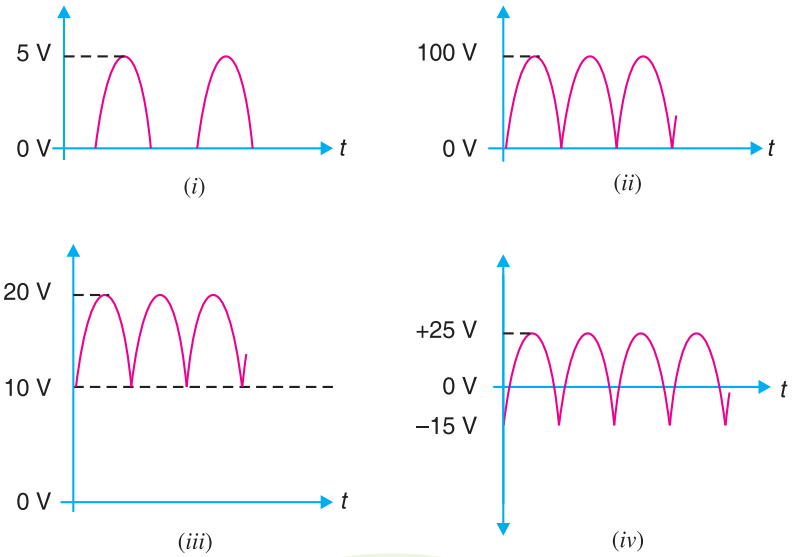


Fig. 6.78

12. Calculate the peak voltage across each half of a centre-tapped transformer used in a full-wave rectifier that has an average output voltage of 110V. **[173V]**

13. What PIV rating is required for the diodes in a bridge rectifier that produces an average output voltage of 50V? **[78.5 V]**

14. In the circuit shown in Fig. 6.79, is zener diode in the on or off state ? **[Off]**

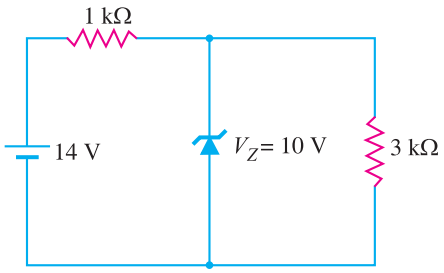


Fig. 6.79

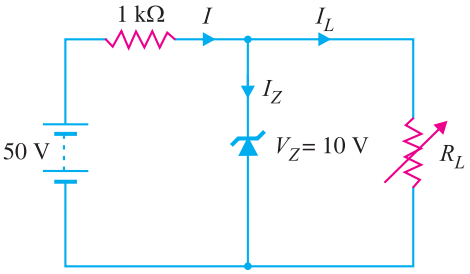


Fig. 6.80

15. In the circuit shown in Fig. 6.80, determine the range of R_L that will result in a constant voltage of 10 V across R_L. **[250 Ω to 1.25 kΩ]**

Discussion Questions

1. Why are diodes not operated in the breakdown region in rectifier service ?
2. Why do we use transformers in rectifier service ?
3. Why is *PIV* important in rectifier service ?
4. Why is zener diode used as a voltage regulator ?
5. Why is capacitor input filter preferred to choke input filter ?

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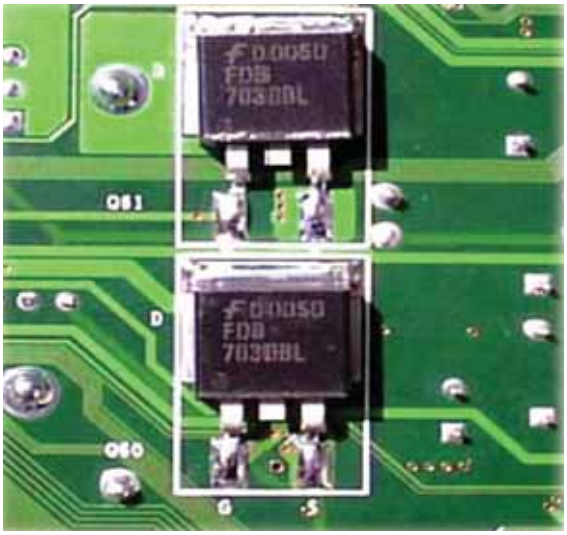
Transistors



INTRODUCTION

When a third doped element is added to a crystal diode in such a way that two *pn* junctions are formed, the resulting device is known as a *transistor*. The transistor—an entirely new type of electronic device—is capable of achieving amplification of weak signals in a fashion comparable and often superior to that realised by vacuum tubes. Transistors are far smaller than vacuum tubes, have no filament and hence need no heating power and may be operated in any position. They are mechanically strong, have practically unlimited life and can do some jobs better than vacuum tubes.

Invented in 1948 by J. Bardeen and W.H. Brattain of Bell Telephone Laboratories, U.S.A.; transistor has now become the heart of most electronic applications. Though transistor is only slightly more than 58 years old, yet it is fast replacing vacuum tubes in almost all applications. In this chapter, we shall focus our attention on the various aspects of transistors and their increasing applications in the fast developing electronics industry.

8.1 Transistor

A **transistor** *consists of two pn junctions formed by* *sandwiching *either p-type or n-type semiconductor between a pair of opposite types.* Accordingly ; there are two types of transistors, namely;

(*i*) *n-p-n* transistor (*ii*) *p-n-p* transistor

An *n-p-n* transistor is composed of two *n*-type semiconductors separated by a thin section of *p*-type as shown in Fig. 8.1 (*i*). However, a *p-n-p* transistor is formed by two *p*-sections separated by a thin section of *n*-type as shown in Fig. 8.1 (*ii*).

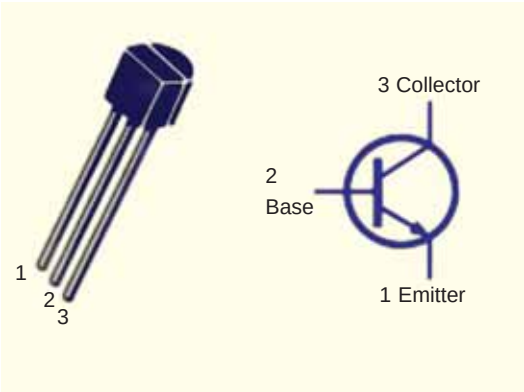
Fig. 8.1

In each type of transistor, the following points may be noted :

(*i*) These are two *pn* junctions. Therefore, a transistor may be regarded as a combination of two diodes connected back to back.

(*ii*) There are three terminals, one taken from each type of semiconductor.

(*iii*) The middle section is a very thin layer. This is the most important factor in the function of a transistor.



Origin of the name "Transistor". When new devices are invented, scientists often try to devise a name that will appropriately describe the device. A transistor has two *pn* junctions. As discussed later, one junction is forward biased and the other is reverse biased. The forward biased junction has a low resistance path whereas a reverse biased junction has a high resistance path. The weak signal is introduced in the low resistance circuit and output is taken from the high resistance circuit. Therefore, a transistor *transfers* a signal from a low resistance to high resistance. The prefix 'trans' means the signal transfer property of the device while 'istor' classifies it as a solid element in the same general family with resistors.

* In practice, these three blocks *p, n, p* are grown out of the same crystal by adding corresponding impurities in turn.

8.2 Naming the Transistor Terminals

A transistor (*pnp* or *npn*) has three sections of doped semiconductors. The section on one side is the *emitter* and the section on the opposite side is the *collector*. The middle section is called the *base* and forms two junctions between the emitter and collector.

(*i*) Emitter. The section on one side that supplies charge carriers (electrons or holes) is called the *emitter*. *The emitter is always forward biased w.r.t. base* so that it can supply a large number of *majority carriers. In Fig. 8.2 (*i*), the emitter (*p*-type) of *pnp* transistor is forward biased and supplies hole charges to its junction with the base. Similarly, in Fig. 8.2 (*ii*), the emitter (*n*-type) of *npn* transistor has a forward bias and supplies free electrons to its junction with the base.

(*ii*) Collector. The section on the other side that collects the charges is called the *collector*. *The collector is always reverse biased*. Its function is to remove charges from its junction with the base. In Fig. 8.2 (*i*), the collector (*p*-type) of *pnp* transistor has a reverse bias and receives hole charges that flow in the output circuit. Similarly, in Fig. 8.2 (*ii*), the collector (*n*-type) of *npn* transistor has reverse bias and receives electrons.

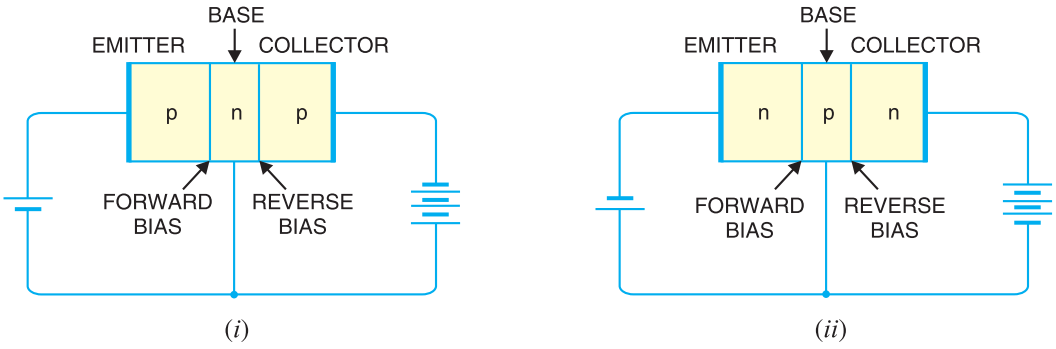


Fig. 8.2

(*iii*) Base. The middle section which forms two *pn*-junctions between the emitter and collector is called the *base*. The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector circuit.

8.3 Some Facts about the Transistor

Before discussing transistor action, it is important that the reader may keep in mind the following facts about the transistor :

(*i*) The transistor has three regions, namely ; *emitter*, *base* and *collector*. The base is much thinner than the emitter while **collector is wider than both as shown in Fig. 8.3. However, for the sake of convenience, it is customary to show emitter and collector to be of equal size.

(*ii*) The emitter is heavily doped so that it can inject a large number of charge carriers (electrons or holes) into the base. The base is lightly doped and very thin ; it passes most of the emitter injected charge carriers to the collector. The collector is moderately doped.

* Holes if emitter is *p*-type and electrons if the emitter is *n*-type.

** During transistor operation, much heat is produced at the collector junction. The collector is made larger to dissipate the heat.

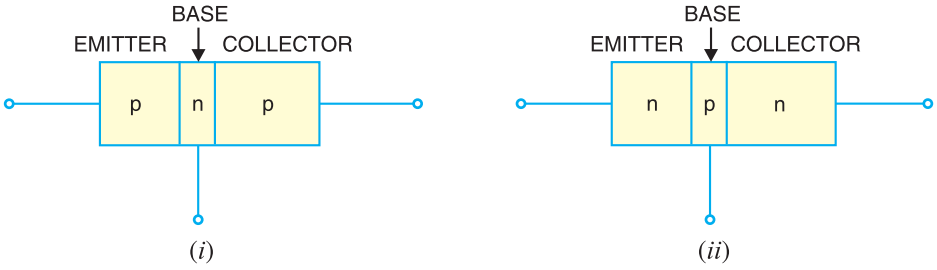


Fig. 8.3

(*iii*) The transistor has two *pn* junctions *i.e.* it is like two diodes. The junction between emitter and base may be called *emitter-base diode* or simply the *emitter diode*. The junction between the base and collector may be called *collector-base diode* or simply *collector diode*.

(*iv*) The emitter diode is always forward biased whereas collector diode is always reverse biased.

(*v*) The resistance of emitter diode (forward biased) is very small as compared to collector diode (reverse biased). Therefore, forward bias applied to the emitter diode is generally very small whereas reverse bias on the collector diode is much higher.

8.4 Transistor Action

The emitter-base junction of a transistor is forward biased whereas collector-base junction is reverse biased. If for a moment, we ignore the presence of emitter-base junction, then *practically** no current would flow in the collector circuit because of the reverse bias. However, if the emitter-base junction is also present, then forward bias on it causes the emitter current to flow. It is seen that this emitter current almost entirely flows in the collector circuit. Therefore, the current in the collector circuit depends upon the emitter current. If the emitter current is zero, then collector current is nearly zero. However, if the emitter current is 1mA, then collector current is also about 1mA. This is precisely what happens in a transistor. We shall now discuss this transistor action for *npn* and *pnp* transistors.

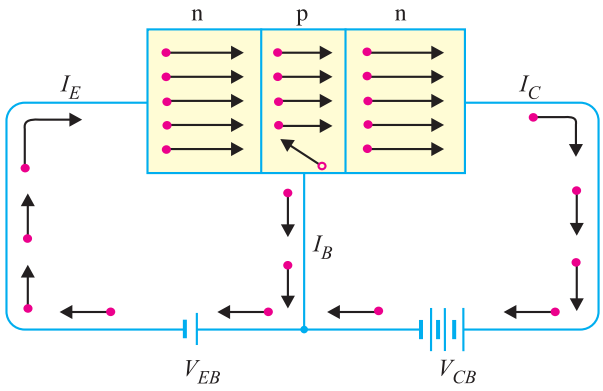
(*i*) Working of npn transistor. Fig. 8.4 shows the *npn* transistor with forward bias to emitter-base junction and reverse bias to collector-base junction. The forward bias causes the electrons in the *n*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the *p*-type base, they tend to combine with holes. As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base** current I_B. The remainder (***more than 95%) cross over into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base currents *i.e.*

$$I_E = I_B + I_C$$

* In actual practice, a very little current (a few μA) would flow in the collector circuit. This is called collector cut off current and is due to minority carriers.

** The electrons which combine with holes become valence electrons. Then as valence electrons, they flow down through holes and into the external base lead. This constitutes base current I_B.

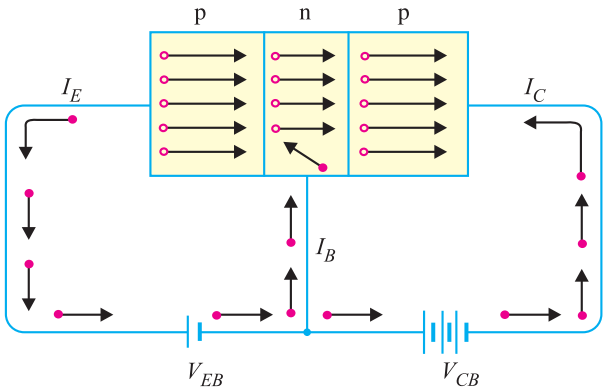
*** The reasons that most of the electrons from emitter continue their journey through the base to collector to form collector current are : (*i*) The base is lightly doped and very thin. Therefore, there are a few holes which find enough time to combine with electrons. (*ii*) The reverse bias on collector is quite high and exerts attractive forces on these electrons.



Basic connection of *npn* transistor

Fig. 8.4

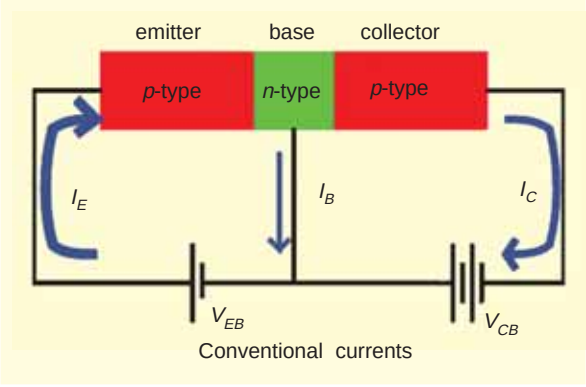
***(ii)* Working of pnp transistor.** Fig. 8.5 shows the basic connection of a *pnp* transistor. The forward bias causes the holes in the *p*-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes cross into *n*-type base, they tend to combine with the electrons. As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the



Basic connection of *pnp* transistor

Fig. 8.5

electrons. The remainder (more than 95%) cross into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It may be noted that current conduction within *pnp* transistor is by holes. However, in the external connecting wires, the current is still by electrons.



Importance of transistor action. The input circuit (*i.e.* emitter-base junction) has low resistance because of forward bias whereas output circuit (*i.e.* collector-base junction) has high resistance due to reverse bias. As we have seen, the input emitter current almost entirely flows in the collector circuit. Therefore, a transistor transfers the input signal current from a low-resistance circuit to a high-resistance circuit. This is the key factor responsible for

the amplifying capability of the transistor. We shall discuss the amplifying property of transistor later in this chapter.

Note. There are two basic transistor types : the **bipolar junction transistor (*BJT*)** and **field-effect transistor** (*FET*). As we shall see, these two transistor types differ in both their operating characteristics and their internal construction. **Note that when we use the term transistor, it means bipolar junction transistor (*BJT*).** The term comes from the fact that in a bipolar transistor, there are *two* types of charge carriers (*viz*. electrons and holes) that play part in conductions. Note that bi means two and polar refers to polarities. The field-effect transistor is simply referred to as *FET*.

8.5 Transistor Symbols

In the earlier diagrams, the transistors have been shown in diagrammatic form. However, for the sake of convenience, the transistors are represented by schematic diagrams. The symbols used for *npn* and *pnp* transistors are shown in Fig. 8.6.

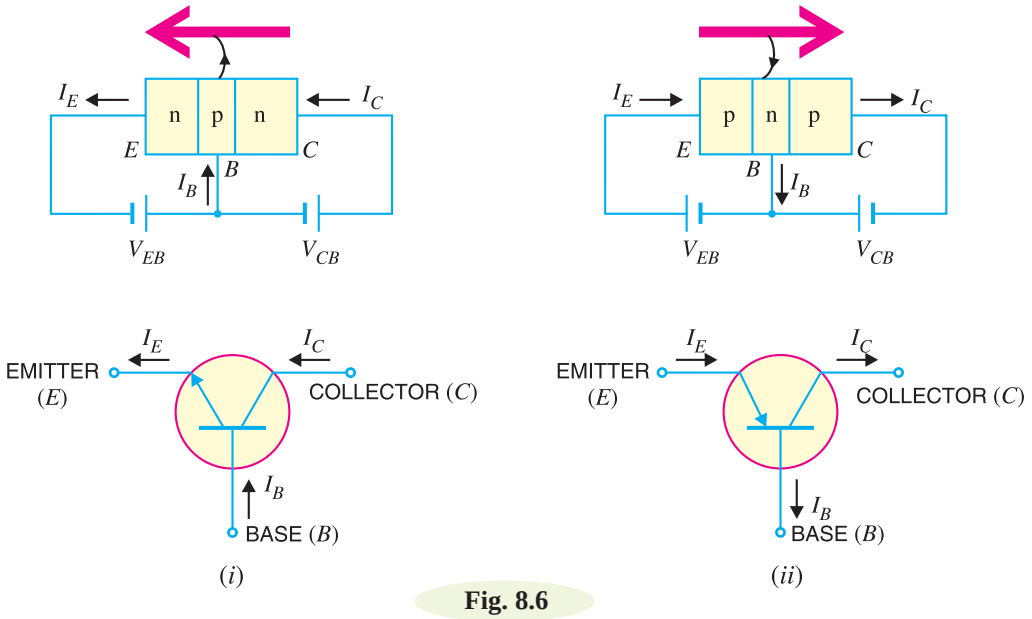


Fig. 8.6

Note that emitter is shown by an arrow which indicates the direction of conventional current flow with forward bias. For *npn* connection, it is clear that conventional current flows out of the emitter as indicated by the outgoing arrow in Fig. 8.6 (*i*). Similarly, for *pnp* connection, the conventional current flows into the emitter as indicated by inward arrow in Fig. 8.6 (*ii*).

8.6 Transistor Circuit as an Amplifier

A transistor raises the strength of a weak signal and thus acts as an amplifier. Fig. 8.7 shows the basic circuit of a transistor amplifier. The weak signal is applied between emitter-base junction and output is taken across the load R_C connected in the collector circuit. In order to achieve faithful amplification, the input circuit should always remain forward biased. To do so, a d.c. voltage V_{EE} is applied in the input circuit in addition to the signal as

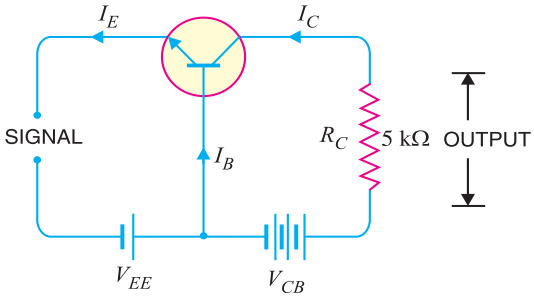


Fig. 8.7

shown. This d.c. voltage is known as bias voltage and its magnitude is such that it always keeps the input circuit forward biased regardless of the polarity of the signal.

As the input circuit has low resistance, therefore, a small change in signal voltage causes an appreciable change in emitter current. This causes almost the *same change in collector current due to transistor action. The collector current flowing through a high load resistance R_C produces a large voltage across it. Thus, a weak signal applied in the input circuit appears in the amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

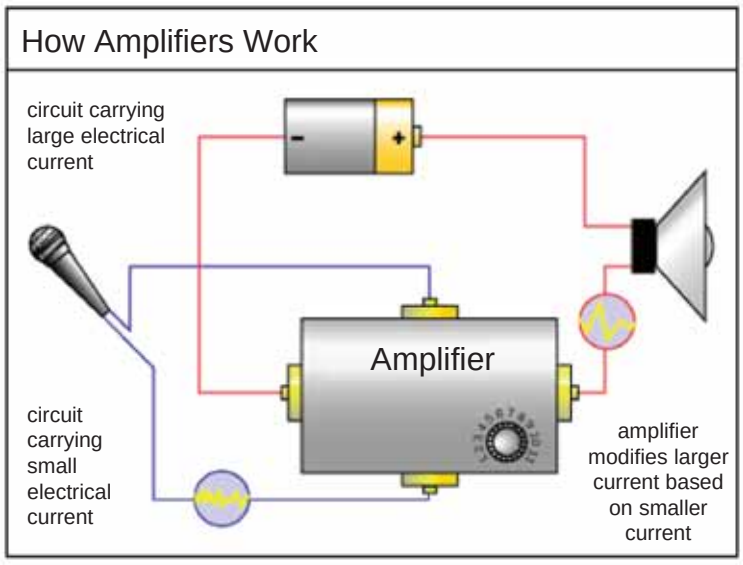


Illustration. The action of a transistor as an amplifier can be made more illustrative if we consider typical circuit values. Suppose collector load resistance R_C = 5 kΩ. Let us further assume that a change of 0.1V in signal voltage produces a change of 1 mA in emitter current. Obviously, the change in collector current would also be approximately 1 mA. This collector current flowing through collector load R_C would produce a voltage = 5 kΩ × 1 mA = 5 V. Thus, a change of 0.1 V in the signal has caused a change of 5 V in the output circuit. In other words, the transistor has been able to raise the voltage level of the signal from 0.1 V to 5 V *i.e.* voltage amplification is 50.

Example 8.1. *A common base transistor amplifier has an input resistance of 20 Ω and output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume* α_{ac} *to be nearly one.*

Solution. **Fig. 8.8 shows the conditions of the problem. Note that output resistance is very high as compared to input resistance. This is not surprising because input junction (base to emitter) of the transistor is forward biased while the output junction (base to collector) is reverse biased.

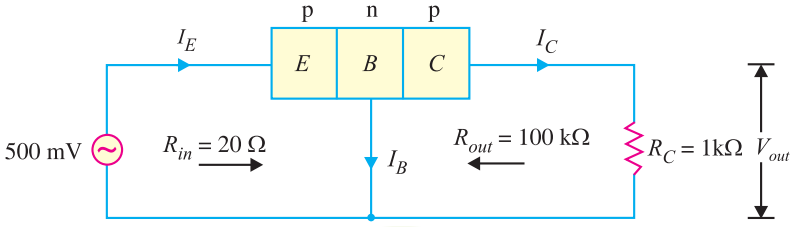


Fig. 8.8

* The reason is as follows. The collector-base junction is reverse biased and has a very high resistance of the order of mega ohms. Thus collector-base voltage has little effect on the collector current. This means that a large resistance R_C can be inserted in series with collector without disturbing the collector current relation to the emitter current *viz.* $I_C = \alpha I_E + I_{CBO}$. Therefore, collector current variations caused by a small base-emitter voltage fluctuations result in voltage changes in R_C that are quite high—often hundreds of times larger than the emitter-base voltage.

** The d.c. biasing is omitted in the figure because our interest is limited to amplification.

Input current, $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500\text{ mV}}{20\ \Omega} = 25$ mA. Since α_{ac} is nearly 1, output current, $I_C = I_E = 25$ mA.

$$\text{Output voltage, } V_{out} = I_C R_C = 25\text{ mA} \times 1\text{ k}\Omega = 25\text{ V}$$

$$\therefore \quad \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25\ V}{500\ mV} = \mathbf{50}$$

Comments. The reader may note that basic amplifying action is produced by transferring a current from a *low-resistance* to a *high-resistance* circuit. Consequently, the name transistor is given to the device by combining the two terms given in magenta letters below :

Transfer + Res**istor** ⟶ **Transistor**

8.7 Transistor Connections

There are three leads in a transistor *viz*., emitter, base and collector terminals. However, when a transistor is to be connected in a circuit, we require four terminals; two for the input and two for the output. This difficulty is overcome by making one terminal of the transistor common to both input and output terminals. The input is fed between this common terminal and one of the other two terminals. The output is obtained between the common terminal and the remaining terminal. Accordingly; a transistor can be connected in a circuit in the following three ways :

(*i*) common base connection **(*ii*)** common emitter connection

(*iii*) common collector connection

Each circuit connection has specific advantages and disadvantages. It may be noted here that regardless of circuit connection, the emitter is always biased in the forward direction, while the collector always has a reverse bias.

8.8 Common Base Connection

In this circuit arrangement, input is applied between emitter and base and output is taken from collector and base. Here, base of the transistor is common to both input and output circuits and hence the name common base connection. In Fig. 8.9 (*i*), a common base *npn* transistor circuit is shown whereas Fig. 8.9 (*ii*) shows the common base *pnp* transistor circuit.

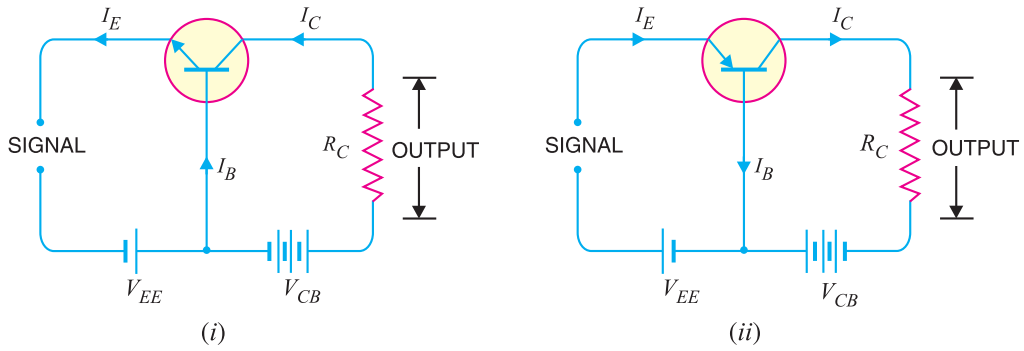


Fig. 8.9

1. Current amplification factor (α). It is the ratio of output current to input current. In a common base connection, the input current is the emitter current I_E and output current is the collector current I_C.

The ratio of change in collector current to the change in emitter current at constant collector-base voltage V_{CB} is known as **current amplification factor** *i.e.*

$$*\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

It is clear that current amplification factor is less than **unity. This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base thin and doping it lightly. Practical values of α in commercial transistors range from 0.9 to 0.99.

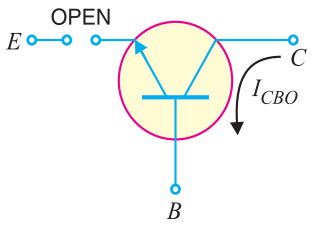


Fig. 8.10

2. Expression for collector current. The whole of emitter current does not reach the collector. It is because a small percentage of it, as a result of electron-hole combinations occurring in base area, gives rise to base current. Moreover, as the collector-base junction is reverse biased, therefore, some leakage current flows due to minority carriers. It follows, therefore, that total collector current consists of :

(i) That part of emitter current which reaches the collector terminal *i.e.* ***αI_E.

(ii) The leakage current $I_{leakage}$. This current is due to the movement of minority carriers across base-collector junction on account of it being reverse biased. This is generally much smaller than αI_E.

$\therefore$ Total collector current, $I_C = \alpha I_E + I_{leakage}$

It is clear that if $I_E = 0$ (*i.e.*, emitter circuit is open), a small leakage current still flows in the collector circuit. This $I_{leakage}$ is abbreviated as I_{CBO}, meaning collector-base current with emitter open. The I_{CBO} is indicated in Fig. 8.10.

$$\therefore \quad I_C = \alpha I_E + I_{CBO} \qquad ...(i)$$

$$\text{Now} \quad I_E = I_C + I_B$$

$$\therefore \quad I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$\text{or} \quad I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$\text{or} \quad I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} \qquad ...(ii)$$

Relation (*i*) or (*ii*) can be used to find I_C. It is further clear from these relations that the collector current of a transistor can be controlled by either the emitter or base current.

Fig. 8.11 shows the concept of I_{CBO}. In *CB* configuration, a small collector current flows even when the emitter current is zero. This is the leakage collector current (*i.e.* the collector current when emitter is open) and is denoted by I_{CBO}. When the emitter voltage V_{EE} is also applied, the various currents are as shown in Fig. 8.11 (*ii*).

Note. Owing to improved construction techniques, the magnitude of I_{CBO} for general-purpose and low-powered transistors (especially silicon transistors) is usually very small and may be neglected in calculations. However, for high power applications, it will appear in microampere range. Further, I_{CBO} is very much temperature dependent; it increases rapidly with the increase in temperature. Therefore, at higher temperatures, I_{CBO} plays an important role and must be taken care of in calculations.

* If only d.c. values are considered, then $\alpha = I_C/I_E$.

** At first sight, it might seem that since there is no current gain, no voltage or power amplification could be possible with this arrangement. However, it may be recalled that output circuit resistance is much higher than the input circuit resistance. Therefore, it does give rise to voltage and power gain.

*** $\alpha = \frac{I_C}{I_E} \quad \therefore \quad I_C = \alpha I_E$

In other words, αI_E part of emitter current reaches the collector terminal.

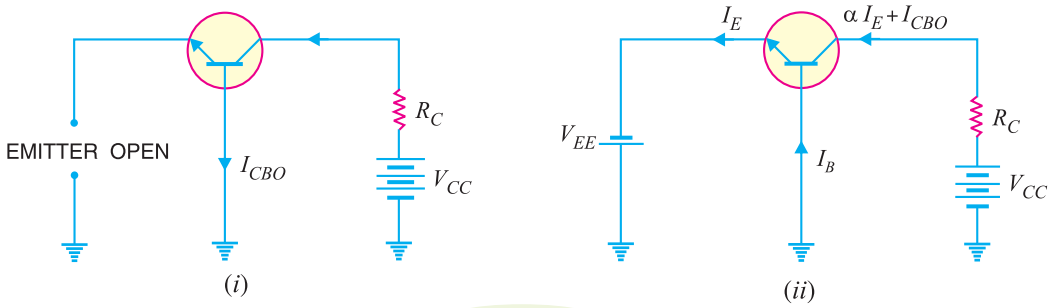


Fig. 8.11

Example 8.2. *In a common base connection, I_E = 1mA, I_C = 0.95mA. Calculate the value of I_B.*

Solution. Using the relation, $I_E = I_B + I_C$

or $1 = I_B + 0.95$

$\therefore$ $I_B = 1 - 0.95 =$ **0.05 mA**

Example 8.3. *In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.*

Solution. Here, $\alpha = 0.9$, $I_E = 1$ mA

Now $\alpha = \dfrac{I_C}{I_E}$

or $I_C = \alpha I_E = 0.9 \times 1 = 0.9$ mA

Also $I_E = I_B + I_C$

$\therefore$ Base current, $I_B = I_E - I_C = 1 - 0.9 =$ **0.1 mA**

Example 8.4. *In a common base connection, I_C = 0.95 mA and I_B = 0.05 mA. Find the value of α.*

Solution. We know $I_E = I_B + I_C = 0.05 + 0.95 = 1$ mA

$\therefore$ Current amplification factor, $\alpha = \dfrac{I_C}{I_E} = \dfrac{0.95}{1} =$ **0.95**

Example 8.5. *In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μA. Find the total collector current. Given that α = 0.92.*

Solution. Here, $I_E = 1$ mA, $\alpha = 0.92$, $I_{CBO} = 50$ μA

$\therefore$ Total collector current, $I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$

$= 0.92 + 0.05 =$ **0.97 mA**

Example 8.6. *In a common base connection, α = 0.95. The voltage drop across 2 kΩ resistance which is connected in the collector is 2V. Find the base current.*

Solution. Fig. 8.12 shows the required common base connection. The voltage drop across R_C (= 2 kΩ) is 2V.

$\therefore$ $I_C = 2$ V/2 kΩ = 1 mA

Now $\alpha = I_C/I_E$

$$\therefore \quad I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05 \text{ mA}$$

Using the relation, $I_E = I_B + I_C$

$$\therefore \quad I_B = I_E - I_C = 1.05 - 1$$

$$= \mathbf{0.05\ mA}$$

Example 8.7. *For the common base circuit shown in Fig. 8.13, determine I_C and V_{CB}. Assume the transistor to be of silicon.*

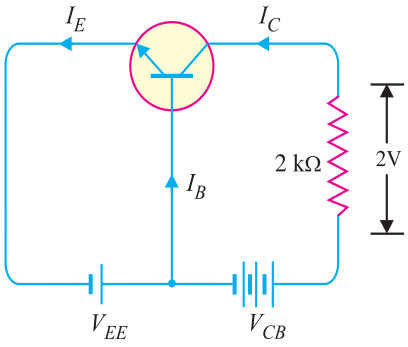


Fig. 8.12

Solution. Since the transistor is of silicon, $V_{BE} = 0.7$V. Applying Kirchhoff's voltage law to the emitter-side loop, we get,

$$V_{EE} = I_E R_E + V_{BE}$$

or $$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{8V - 0.7V}{1.5\ \text{k}\Omega} = 4.87 \text{ mA}$$

$$\therefore \quad I_C \simeq I_E = \mathbf{4.87\ mA}$$

Applying Kirchhoff's voltage law to the collector-side loop, we have,

$$V_{CC} = I_C R_C + V_{CB}$$

$$\therefore \quad V_{CB} = V_{CC} - I_C R_C$$

$$= 18 \text{ V} - 4.87 \text{ mA} \times 1.2\ \text{k}\Omega = \mathbf{12.16\ V}$$

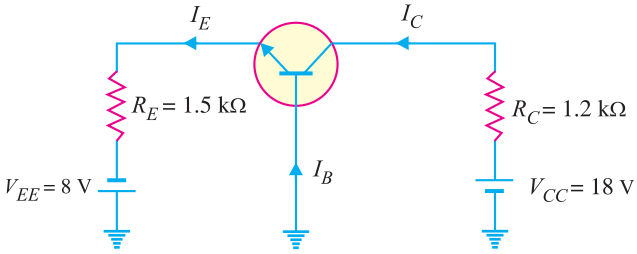


Fig. 8.13

8.9 Characteristics of Common Base Connection

The complete electrical behaviour of a transistor can be described by stating the interrelation of the various currents and voltages. These relationships can be conveniently displayed graphically and the curves thus obtained are known as the characteristics of transistor. The most important characteristics of common base connection are *input characteristics* and *output characteristics*.

1. Input characteristic. It is the curve between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The emitter current is generally taken along *y*-axis and emitter-base voltage along *x*-axis. Fig. 8.14 shows the input characteristics of a typical transistor in *CB* arrangement . The following points may be noted from these characteristics :

(i) The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. It means that input resistance is very small.

(ii) The emitter current is almost independent of collector-base voltage V_{CB}. This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.

Input resistance. It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting

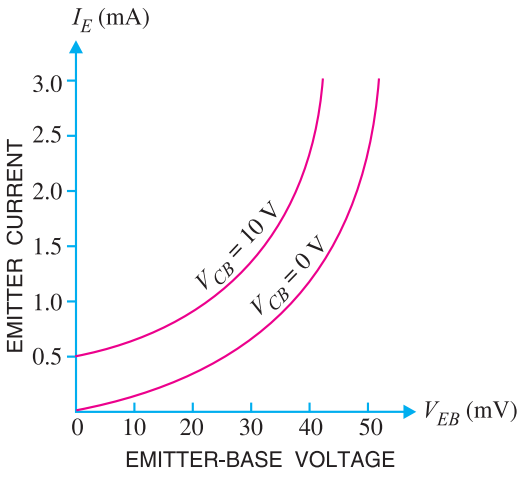


Fig. 8.14

change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) *i.e.*

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_E} \text{ at constant } V_{CB}$$

In fact, input resistance is the opposition offered to the signal current. As a very small V_{EB} is sufficient to produce a large flow of emitter current I_E, therefore, input resistance is quite small, of the order of a few ohms.

2. Output characteristic. It is the curve between collector current I_C and collector-base voltage V_{CB} at *constant emitter current I_E. Generally, collector current is taken along *y*-axis and collector-base voltage along *x*-axis. Fig. 8.15 shows the output characteristics of a typical transistor in *CB* arrangement.

The following points may be noted from the characteristics :

(*i*) The collector current I_C varies with V_{CB} only at very low voltages (< 1V). The transistor is *never* operated in this region.

(*ii*) When the value of V_{CB} is raised above 1 – 2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon I_E only. This is consistent with the theory that the emitter current flows *almost* entirely to the collector terminal. The transistor is *always* operated in this region.

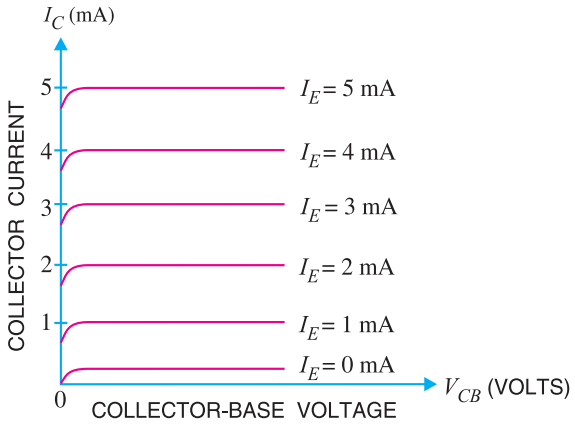


Fig. 8.15

(*iii*) A very large change in collector-base voltage produces only a tiny change in collector current. This means that output resistance is very high.

Output resistance. It is the ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

The output resistance of *CB* circuit is very high, of the order of several tens of kilo-ohms. This is not surprising because the collector current changes very slightly with the change in V_{CB}.

8.10 Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter. Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter connection. Fig. 8.16 (*i*) shows common emitter *npn* transistor circuit whereas Fig. 8.16 (*ii*) shows common emitter *pnp* transistor circuit.

* I_E has to be kept constant because any change in I_E will produce corresponding change in I_C. Here, we are interested to see how V_{CB} influences I_C.

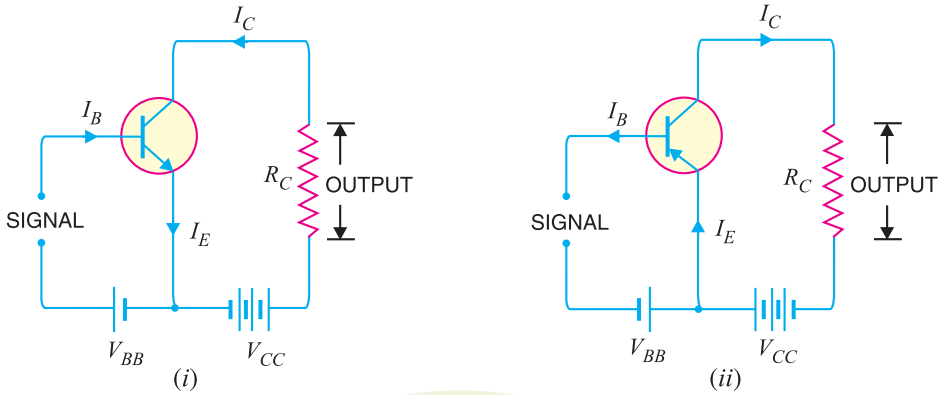


Fig. 8.16

1. Base current amplification factor (β). In common emitter connection, input current is I_B and output current is I_C.

The ratio of change in collector current (ΔI_C) *to the change in base current* (ΔI_B) *is known as* **base current amplification factor** *i.e.*

$$\beta^* = \frac{\Delta I_C}{\Delta I_B}$$

In almost any transistor, less than 5% of emitter current flows as the base current. Therefore, the value of β is generally greater than 20. Usually, its value ranges from 20 to 500. This type of connection is frequently used as it gives appreciable current gain as well as voltage gain.

Relation between β and α. A simple relation exists between β and α. This can be derived as follows :

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad ...(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad ...(ii)$$

Now $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \quad ...(iii)$$

Dividing the numerator and denominator of R.H.S. of exp. (*iii*) by ΔI_E, we get,

$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha} \qquad \left[\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right]$$

$$\therefore \quad \beta = \frac{\alpha}{1-\alpha}$$

It is clear that as α approaches unity, β approaches infinity. In other words, the current gain in common emitter connection is very high. It is due to this reason that this circuit arrangement is used in about 90 to 95 percent of all transistor applications.

* If d.c. values are considered, $\beta = I_C/I_B$.

2. Expression for collector current. In common emitter circuit, I_B is the input current and I_C is the output current.

$$\text{We know } I_E = I_B + I_C \quad ...(i)$$

$$\text{and } I_C = \alpha I_E + I_{CBO} \quad ...(ii)$$

$$\text{From exp. } (ii), \text{ we get, } I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

$$\text{or } I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$\text{or } I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \quad ...(iii)$$

From exp. (*iii*), it is apparent that if $I_B = 0$ (*i.e.* base circuit is open), the collector current will be the current to the emitter. This is abbreviated as I_{CEO}, meaning collector-emitter current with base open.

$$\therefore I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

Substituting the value of $\frac{1}{1-\alpha} I_{CBO} = I_{CEO}$ in exp. (*iii*), we get,

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

$$\text{or } I_C = \beta I_B + I_{CEO} \qquad \left(\because \beta = \frac{\alpha}{1-\alpha}\right)$$

Concept of I_{CEO}. In *CE* configuration, a small collector current flows even when the base current is zero [See Fig. 8.17 (*i*)]. This is the collector cut off current (*i.e.* the collector current that flows when base is open) and is denoted by I_{CEO}. The value of I_{CEO} is much larger than I_{CBO}.

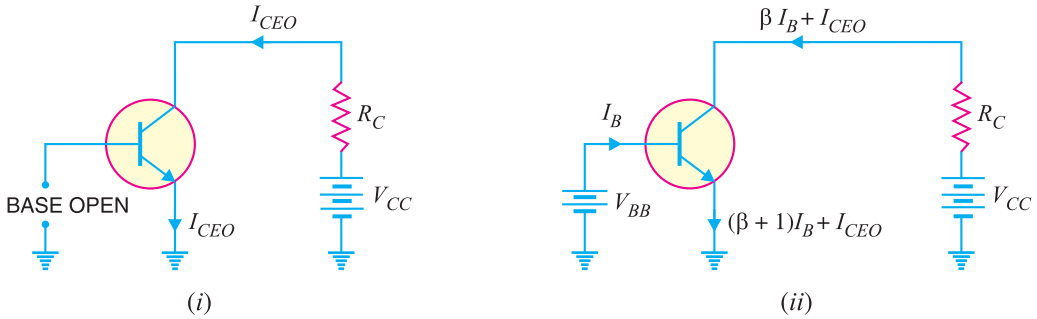


Fig. 8.17

When the base voltage is applied as shown in Fig. 8.17 (*ii*), then the various currents are :

$$\text{Base current} = I_B$$

$$\text{Collector current} = \beta I_B + I_{CEO}$$

$$\text{Emitter current} = \text{Collector current} + \text{Base current}$$

$$= (\beta I_B + I_{CEO}) + I_B = (\beta + 1) I_B + I_{CEO}$$

It may be noted here that :

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO} = (\beta + 1) I_{CBO} \qquad \left[\because \frac{1}{1-\alpha} = \beta + 1\right]$$

8.11. Measurement of Leakage Current

A very small leakage current flows in all transistor circuits. However, in most cases, it is quite small and can be neglected.

***(i)* Circuit for I_{CEO} test.** Fig. 8.18 shows the circuit for measuring I_{CEO}. Since base is open

($I_B = 0$), the transistor is in cut off. Ideally, $I_C = 0$ but actually there is a small current from collector to emitter due to minority carriers. It is called I_{CEO} (collector-to-emitter current with base open). This current is usually in the nA range for silicon. A faulty transistor will often have excessive leakage current.

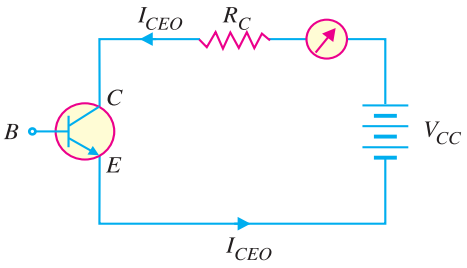


Fig. 8.18

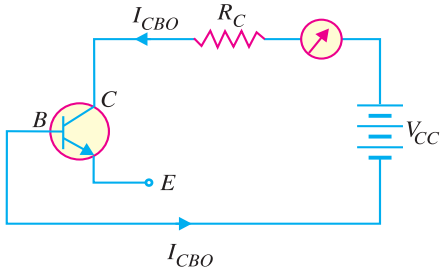


Fig. 8.19

***(ii)* Circuit for I_{CBO} test.** Fig. 8.19 shows the circuit for measuring I_{CBO}. Since the emitter is open ($I_E = 0$), there is a small current from collector to base. This is called I_{CBO} (collector-to-base current with emitter open). This current is due to the movement of minority carriers across base-collector junction. The value of I_{CBO} is also small. If in measurement, I_{CBO} is excessive, then there is a possibility that collector-base is shorted.

Example 8.8. *Find the value of β if (i) α = 0.9 (ii) α = 0.98 (iii) α = 0.99.*

Solution. ***(i)*** $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.9}{1-0.9} = \mathbf{9}$

(ii) $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.98}{1-0.98} = \mathbf{49}$

(iii) $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.99}{1-0.99} = \mathbf{99}$

Example 8.9. *Calculate I_E in a transistor for which β = 50 and I_B = 20 μA.*

Solution. Here $\beta = 50, \quad I_B = 20\mu A = 0.02$ mA

Now $\beta = \dfrac{I_C}{I_B}$

$\therefore \quad I_C = \beta I_B = 50 \times 0.02 = 1$ mA

Using the relation, $I_E = I_B + I_C = 0.02 + 1 = \mathbf{1.02\ mA}$

Example 8.10. *Find the α rating of the transistor shown in Fig. 8.20. Hence determine the value of I_C using both α and β rating of the transistor.*

Solution. Fig. 8.20 shows the conditions of the problem.

$$\alpha = \frac{\beta}{1+\beta} = \frac{49}{1+49} = \mathbf{0.98}$$

The value of I_C can be found by using either α or β rating as under :

$I_C = \alpha I_E = 0.98\ (12\ \text{mA}) = \mathbf{11.76\ mA}$

Also $I_C = \beta I_B = 49\ (240\ \mu\text{A}) = \mathbf{11.76\ mA}$

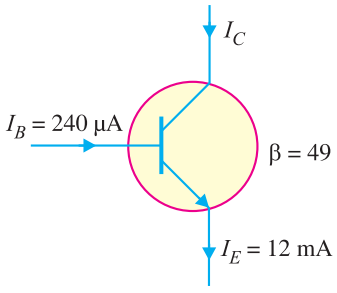


Fig. 8.20

Example 8.11. *For a transistor, β = 45 and voltage drop across 1kΩ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.*

Solution. Fig. 8.21 shows the required common emitter connection. The voltage drop across R_C (= 1 kΩ) is 1volt.

$$\therefore \quad I_C = \frac{1\,V}{1\,k\Omega} = 1 \text{ mA}$$

$$\text{Now} \quad \beta = \frac{I_C}{I_B}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{1}{45} = \mathbf{0.022\ mA}$$

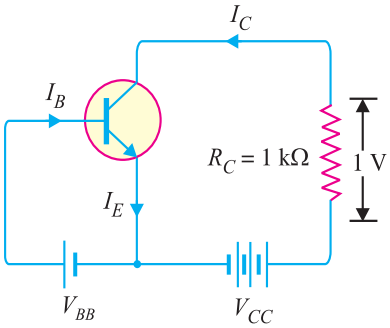


Fig. 8.21

Example 8.12. *A transistor is connected in common emitter (CE) configuration in which collector supply is 8V and the voltage drop across resistance R_C connected in the collector circuit is 0.5V. The value of R_C = 800 Ω. If α = 0.96, determine :*

(i) collector-emitter voltage

(ii) base current

Solution. Fig. 8.22 shows the required common emitter connection with various values.

(*i*) Collector-emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = \mathbf{7.5\ V}$$

(*ii*) The voltage drop across R_C (= 800 Ω) is 0.5 V.

$$\therefore \quad I_C = \frac{0.5\text{ V}}{800\ \Omega} = \frac{5}{8}\text{ mA} = 0.625\text{ mA}$$

$$\text{Now} \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24$$

$$\therefore \text{ Base current, } I_B = \frac{I_C}{\beta} = \frac{0.625}{24} = \mathbf{0.026\ mA}$$

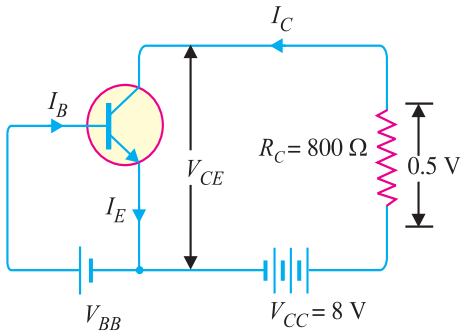


Fig. 8.22

Example 8.13. *An n-p-n transistor at room temperature has its emitter disconnected. A voltage of 5V is applied between collector and base. With collector positive, a current of 0.2 μA flows. When the base is disconnected and the same voltage is applied between collector and emitter, the current is found to be 20 μA. Find α, I_E and I_B when collector current is 1mA.*

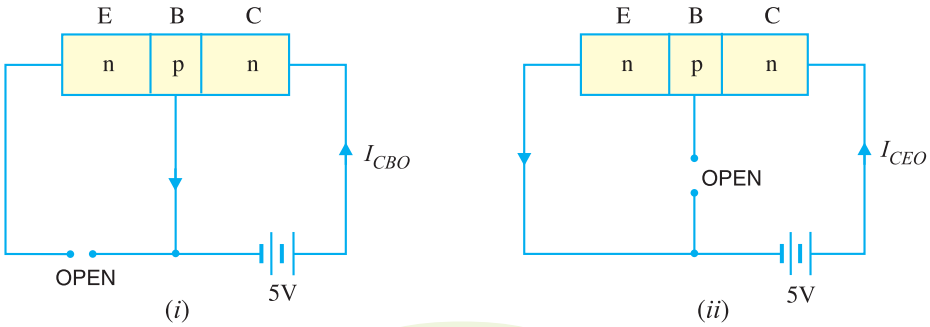


Fig. 8.23

Solution. When the emitter circuit is open [See Fig. 8.23 (*i*)], the collector-base junction is reverse biased. A small leakage current I_{CBO} flows due to minority carriers.

$\therefore \quad I_{CBO} = 0.2\ \mu A$ ...*given*

When base is open [See Fig. 8.23 (*ii*)], a small leakage current I_{CEO} flows due to minority carriers.

$\therefore \quad I_{CEO} = 20\ \mu A$ ... *given*

We know $\quad I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}$

or $\quad 20 = \dfrac{0.2}{1-\alpha}$

$\therefore \quad \alpha = \mathbf{0.99}$

Now $\quad I_C = \alpha I_E + I_{CBO}$

Here $\quad I_C = 1\text{mA} = 1000\ \mu\text{A}\ ;\ \alpha = 0.99\ ;\ I_{CBO} = 0.2\ \mu\text{A}$

$\therefore \quad 1000 = 0.99 \times I_E + 0.2$

or $\quad I_E = \dfrac{1000 - 0.2}{0.99} = \mathbf{1010\ \mu A}$

and $\quad I_B = I_E - I_C = 1010 - 1000 = \mathbf{10\ \mu A}$

Example 8.14. *The collector leakage current in a transistor is 300 μA in CE arrangement. If now the transistor is connected in CB arrangement, what will be the leakage current? Given that β = 120.*

Solution. $I_{CEO} = 300\ \mu A$

$$\beta = 120\ ;\ \alpha = \frac{\beta}{\beta+1} = \frac{120}{120+1} = 0.992$$

Now, $\quad I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}$

$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.992) \times 300 = \mathbf{2.4\ \mu A}$

Note that leakage current in *CE* arrangement (*i.e.* I_{CEO}) is much more than in *CB* arrangement (*i.e.* I_{CBO}).

Example 8.15. *For a certain transistor, I_B = 20 μA; I_C = 2 mA and β = 80. Calculate I_{CBO}.*

Solution.

$$I_C = \beta I_B + I_{CEO}$$

or $\quad 2 = 80 \times 0.02 + I_{CEO}$

$\therefore \quad I_{CEO} = 2 - 80 \times 0.02 = 0.4\ \text{mA}$

Now $\quad \alpha = \dfrac{\beta}{\beta+1} = \dfrac{80}{80+1} = 0.988$

$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.988) \times 0.4 = \mathbf{0.0048\ mA}$

Example 8.16. *Using diagrams, explain the correctness of the relation $I_{CEO} = (\beta + 1)\, I_{CBO}$.*

Solution. The leakage current I_{CBO} is the current that flows through the base-collector junction when emitter is open as shown is Fig. 8.24. When the transistor is in *CE* arrangement, the *base current (*i.e.* I_{CBO}) is multiplied by β in the collector as shown in Fig. 8.25.

$\therefore \quad I_{CEO} = I_{CBO} + \beta I_{CBO} = (\beta + 1)\, I_{CBO}$

* The current I_{CBO} is amplified because it is forced to flow across the base-emitter junction.

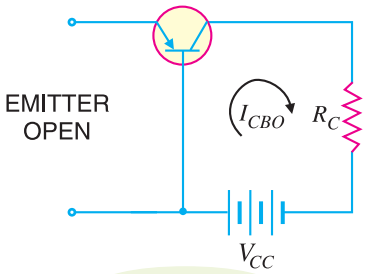


Fig. 8.24

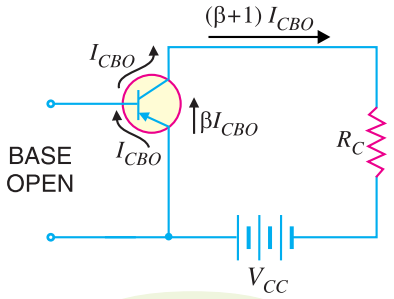


Fig. 8.25

Example 8.17 *Determine V_{CB} in the transistor * circuit shown in Fig. 8.26 (i). The transistor is of silicon and has $\beta = 150$.*

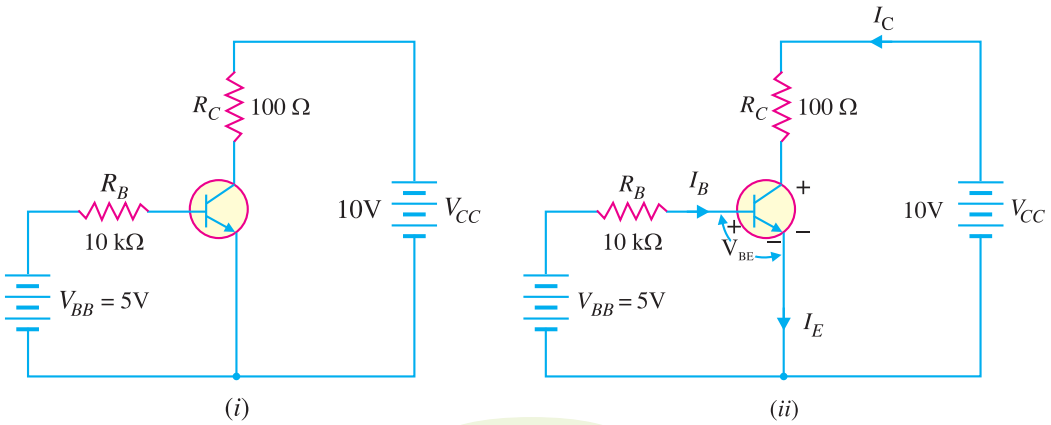


Fig. 8.26

Solution. Fig. 8.26 (*i*) shows the transistor circuit while Fig. 8.26 (*ii*) shows the various currents and voltages along with polarities.

Applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or $$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{10\, k\Omega} = 430\ \mu A$$

$\therefore$ $$I_C = \beta I_B = (150)(430\ \mu A) = 64.5\ mA$$

Now $$V_{CE} = V_{CC} - I_C R_C$$

$$= 10V - (64.5\ mA)\ (100\Omega) = 10V - 6.45V = 3.55V$$

We know that : $$V_{CE} = V_{CB} + V_{BE}$$

$\therefore$ $$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = \mathbf{2.85V}$$

Example 8.18. *In a transistor, $I_B = 68\ \mu A$, $I_E = 30\ mA$ and $\beta = 440$. Determine the α rating of the transistor. Then determine the value of I_C using both the α rating and β rating of the transistor.*

Solution.

$$\alpha = \frac{\beta}{\beta + 1} = \frac{440}{440 + 1} = \mathbf{0.9977}$$

* The resistor R_B controls the base current I_B and hence collector current I_C ($= \beta I_B$). If R_B is increased, the base current (I_B) decreases and hence collector current (I_C) will decrease and vice-versa.

$$I_C = \alpha I_E = (0.9977)\ (30\ \text{mA}) = \mathbf{29.93\ mA}$$

Also $$I_C = \beta I_B = (440)\ (68\ \mu\text{A}) = \mathbf{29.93\ mA}$$

Example 8.19. *A transistor has the following ratings : $I_{C\,(max)}$ = 500 mA and β_{max} = 300. Determine the maximum allowable value of I_B for the device.*

Solution.

$$I_{B\,(max)} = \frac{I_{C\,(max)}}{\beta_{max}} = \frac{500\ \text{mA}}{300} = \mathbf{1.67\ mA}$$

For this transistor, if the base current is allowed to exceed 1.67 mA, the collector current will exceed its maximum rating of 500 mA and the transistor will probably be destroyed.

Example 8.20. *Fig. 8.27 shows the open circuit failures in a transistor. What will be the circuit behaviour in each case ?*

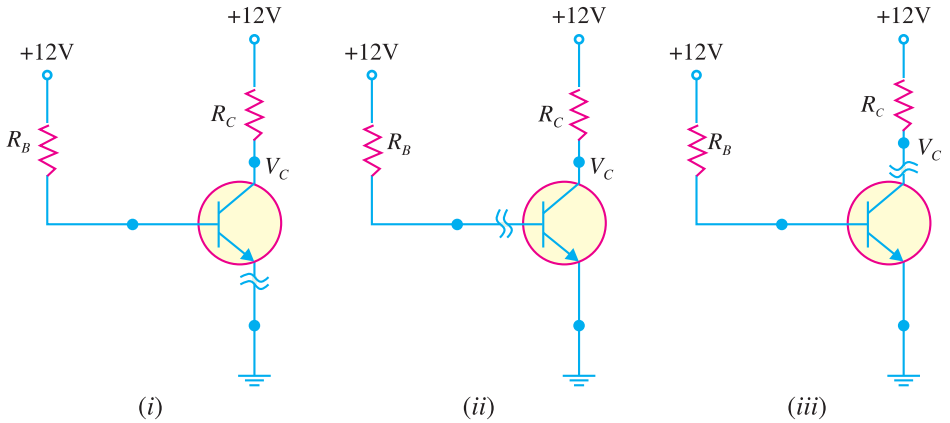


Fig. 8.27

Solution. *Fig 8.27 shows the open circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) Open emitter. Fig. 8.27 (*i*) shows an open emitter failure in a transistor. Since the collector diode is not forward biased, it is *OFF* and there can be neither collector current nor base current. Therefore, there will be no voltage drops across either resistor and the voltage at the base and at the collector leads of the transistor will be 12V.

(*ii*) Open-base. Fig. 8.27 (*ii*) shows an open base failure in a transistor. Since the base is open, there can be no base current so that the transistor is in *cut-off*. Therefore, all the transistor currents are 0A. In this case, the base and collector voltages will both be at 12V.

Note. It may be noted that an open failure at either the base or emitter will produce similar results.

(*iii*) Open collector. Fig. 8.27 (*iii*) shows an open collector failure in a transistor. In this case, the emitter diode is still *ON*, so we expect to see 0.7V at the base. However, we will see 12V at the collector because there is no collector current.

Example 8.21. *Fig. 8.28 shows the short circuit failures in a transistor. What will be the circuit behaviour in each case ?*

* The collector resistor R_C controls the collector voltage V_C (= $V_{CC} - I_C R_C$). When R_C increases, V_C decreases and vice-versa.

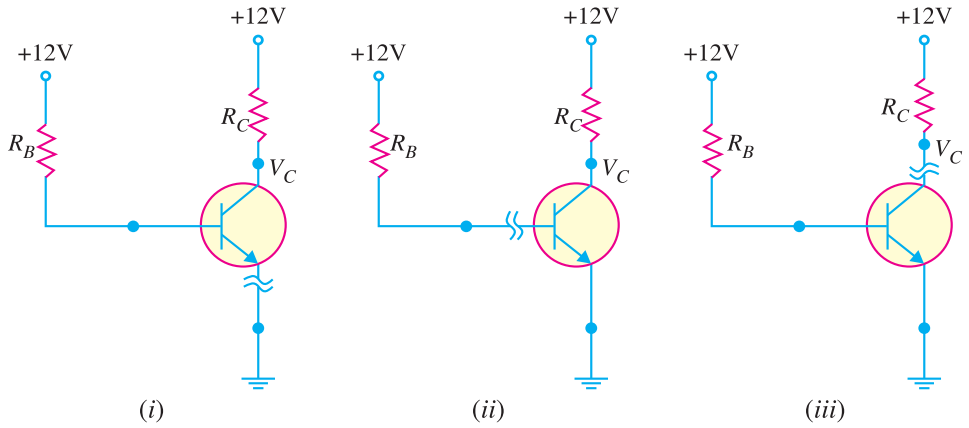


Fig. 8.28

Solution. Fig. 8.28 shows the short circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) Collector-emitter short. Fig. 8.28 (*i*) shows a short between collector and emitter. The emitter diode is still forward biased, so we expect to see 0.7V at the base. Since the collector is shorted to the emitter, $V_C = V_E = 0$V.

(*ii*) Base -emitter short. Fig 8.28 (*ii*) shows a short between base and emitter. Since the base is now directly connected to ground, $V_B = 0$. Therefore, the current through R_B will be diverted to ground and there is no current to forward bias the emitter diode. As a result, the transistor will be *cut-off* and there is no collector current. So we will expect the collector voltage to be 12V.

(*iii*) Collector-base short. Fig. 8.28 (*iii*) shows a short between the collector and the base. In this case, the emitter diode is still forward biased so $V_B = 0.7$V. Now, however, because the collector is shorted to the base, $V_C = V_B = 0.7$V.

Note. The collector-emitter short is probably the most common type of fault in a transistor. It is because the collector current (I_C) and collector-emitter voltage (V_{CE}) are responsible for the major part of the power dissipation in the transistor. As we shall see (See Art. 8.23), the power dissipation in a transistor is mainly due to I_C and V_{CE} (*i.e.* $P_D = V_{CE}\, I_C$). Therefore, the transistor chip between the collector and the emitter is most likely to melt first.

8.12 Characteristics of Common Emitter Connection

The important characteristics of this circuit arrangement are the *input characteristics* and *output characteristics*.

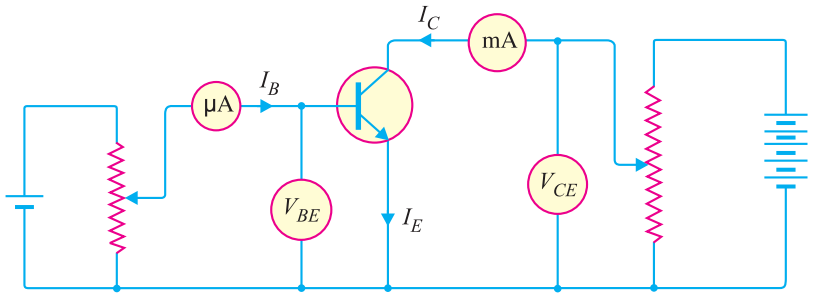


Fig. 8.29

1. Input characteristic. *It is the curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.*

The input characteristics of a *CE* connection can be determined by the circuit shown in Fig. 8.29. Keeping V_{CE} constant (say at 10 V), note the base current I_B for various values of V_{BE}. Then plot the readings obtained on the graph, taking I_B along *y*-axis and V_{BE} along *x*-axis. This gives the input characteristic at V_{CE} = 10V as shown in Fig. 8.30. Following a similar procedure, a family of input characteristics can be drawn. The following points may be noted from the characteristics :

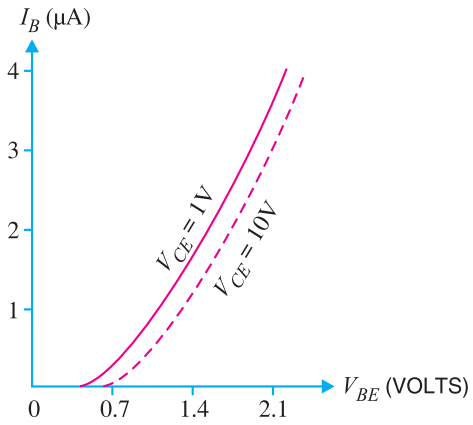


Fig. 8.30

(*i*) The characteristic resembles that of a forward biased diode curve. This is expected since the base-emitter section of transistor is a diode and it is forward biased.

(*ii*) As compared to *CB* arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a *CE* circuit is higher than that of *CB* circuit.

Input resistance. It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE} *i.e.*

$$\text{Input resistance,} \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{at constant } V_{CE}$$

The value of input resistance for a *CE* circuit is of the order of a few hundred ohms.

2. Output characteristic. *It is the curve between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B.*

The output characteristics of a *CE* circuit can be drawn with the help of the circuit shown in Fig. 8.29. Keeping the base current I_B fixed at some value say, 5 μA, note the collector current I_C for various values of V_{CE}. Then plot the readings on a graph, taking I_C along *y*-axis and V_{CE} along *x*-axis. This gives the output characteristic at I_B = 5 μA as shown in Fig. 8.31 (*i*). The test can be repeated for I_B = 10 μA to obtain the new output characteristic as shown in Fig. 8.31 (*ii*). Following similar procedure, a family of output characteristics can be drawn as shown in Fig. 8.31 (*iii*).

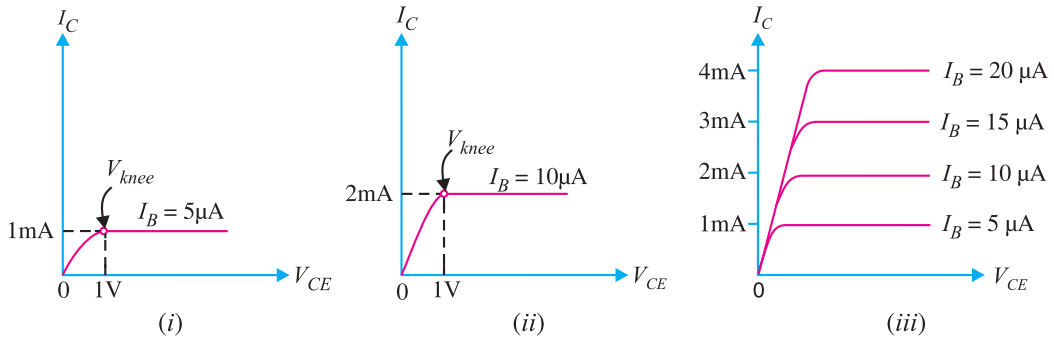


Fig. 8.31

The following points may be noted from the characteristics:

(*i*) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, collector current becomes *almost* constant and independent of V_{CE}. This value of V_{CE} upto which collector

current I_C changes with V_{CE} is called the *knee voltage* (V_{knee}). *The transistors are always operated in the region above knee voltage.*

(ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.

(iii) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$.

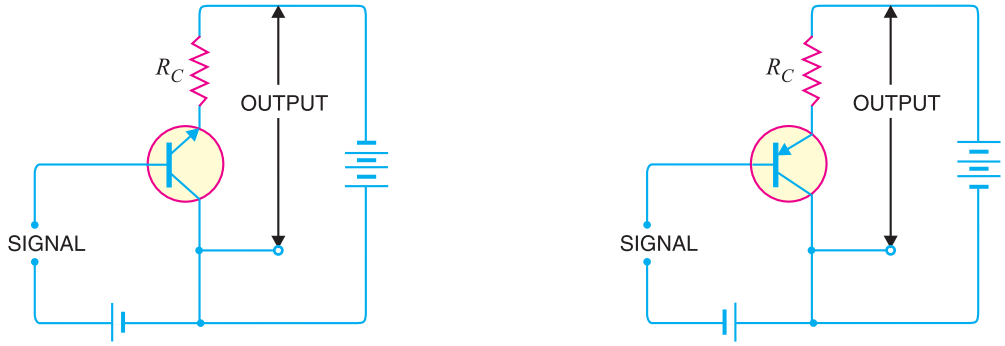
Output resistance. It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

It may be noted that whereas the output characteristics of *CB* circuit are horizontal, they have noticeable slope for the *CE* circuit. Therefore, the output resistance of a *CE* circuit is less than that of *CB* circuit. Its value is of the order of 50 kΩ.

8.13 Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector. Here, collector of the transistor is common to both input and output circuits and hence the name common collector connection. Fig. 8.32 (*i*) shows common collector *npn* transistor circuit whereas Fig. 8.32 (*ii*) shows common collector *pnp* circuit.



(*i*) (*ii*)

Fig. 8.32

***(i)* Current amplification factor γ.** In common collector circuit, input current is the base current I_B and output current is the emitter current I_E. Therefore, current amplification in this circuit arrangement can be defined as under :

The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as **current amplification factor** *in common collector (CC) arrangement i.e.*

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

This circuit provides about the same current gain as the common emitter circuit as $\Delta I_E \simeq \Delta I_C$. However, its voltage gain is always less than 1.

Relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \qquad ...(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad ...(ii)$$

Now $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator of R.H.S. by ΔI_E, we get,

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \qquad \left(\text{Q } \alpha = \frac{\Delta I_C}{\Delta I_E}\right)$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha}$$

(*ii*) Expression for collector current

We know $I_C = \alpha I_E + I_{CBO}$ (See Art. 8.8)

Also $I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$

$\therefore \quad I_E (1-\alpha) = I_B + I_{CBO}$

or $I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$

or $I_C \; ; \; I_E = *(\beta + 1) I_B + (\beta + 1) I_{CBO}$

(*iii*) Applications. The common collector circuit has very high input resistance (about 750 kΩ) and very low output resistance (about 25 Ω). Due to this reason, the voltage gain provided by this circuit is always less than 1. Therefore, this circuit arrangement is seldom used for amplification. However, due to relatively high input resistance and low output resistance, this circuit is primarily used for impedance matching *i.e.* for driving a low impedance load from a high impedance source.

8.14 Comparison of Transistor Connections

The comparison of various characteristics of the three connections is given below in the tabular form.

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

The following points are worth noting about transistor arrangements :

* $\beta = \frac{\alpha}{1-\alpha} \quad \therefore \quad \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha}$

(*i*) CB Circuit. The input resistance (r_i) of *CB* circuit is low because I_E is high. The output resistance (r_o) is high because of reverse voltage at the collector. It has no current gain ($\alpha < 1$) but voltage gain can be high. The *CB* circuit is seldom used. The only advantage of *CB* circuit is that it provides good stability against increase in temperature.

(*ii*) CE Circuit. The input resistance (r_i) of a *CE* circuit is high because of small I_B. Therefore, r_i for a *CE* circuit is much higher than that of *CB* circuit. The output resistance (r_o) of *CE* circuit is smaller than that of *CB* circuit. The current gain of *CE* circuit is large because I_C is much larger than I_B. The voltage gain of *CE* circuit is larger than that of *CB* circuit. The *CE* circuit is generally used because it has the best combination of voltage gain and current gain. The disadvantage of *CE* circuit is that the leakage current is amplified in the circuit, but bias stabilisation methods can be used.

(*iii*) CC Circuit. The input resistance (r_i) and output resistance (r_o) of *CC* circuit are respectively high and low as compared to other circuits. There is no voltage gain ($A_v < 1$) in a *CC* circuit. This circuit is often used for impedance matching.

8.15 Commonly Used Transistor Connection

Out of the three transistor connections, the common emitter circuit is the most efficient. It is used in about 90 to 95 per cent of all transistor applications. The main reasons for the widespread use of this circuit arrangement are :

(*i*) High current gain. In a common emitter connection, I_C is the output current and I_B is the input current. In this circuit arrangement, collector current is given by :

$$I_C = \beta I_B + I_{CEO}$$

As the value of β is very large, therefore, the output current I_C is much more than the input current I_B. Hence, the current gain in *CE* arrangement is very high. It may range from 20 to 500.

(*ii*) High voltage and power gain. Due to high current gain, the common emitter circuit has the highest voltage and power gain of three transistor connections. This is the major reason for using the transistor in this circuit arrangement.

(*iii*) Moderate output to input impedance ratio. In a common emitter circuit, the ratio of output impedance to input impedance is small (about 50). This makes this circuit arrangement an ideal one for coupling between various transistor stages. However, in other connections, the ratio of output impedance to input impedance is very large and hence coupling becomes highly inefficient due to gross mismatching.

8.16 Transistor as an Amplifier in *CE* Arrangement

Fig. 8.33 shows the common emitter *npn* amplifier circuit. Note that a battery V_{BB} is connected in the input circuit in addition to the signal voltage. This d.c. voltage is known as *bias voltage* and its magnitude is such that it always keeps the emitter-base junction forward *biased regardless of the polarity of the signal source.

Operation. During the positive half-cycle of the **signal, the forward bias across the emitter-base junction is increased. Therefore, more electrons flow from the emitter to the collector *via* the base. This causes an increase in collector current. The increased collector current produces a greater voltage drop across the collector load resistance R_C. However, during the negative half-cycle of the

* If d.c. bias voltage is not provided, then during negative half-cycle of the signal, the emitter-base junction will be reverse biased. This will upset the transistor action.

** Throughout the book, we shall use sine wave signals because these are convenient for testing amplifiers. But it must be realised that signals (*e.g.* speech, music etc.) with which we work are generally complex having little resemblance to a sine wave. However, fourier series analysis tells us that such complex signals may be expressed as a sum of sine waves of various frequencies.

signal, the forward bias across emitter-base junction is decreased. Therefore, collector current decreases. This results in the decreased output voltage (in the opposite direction). Hence, an amplified output is obtained across the load.

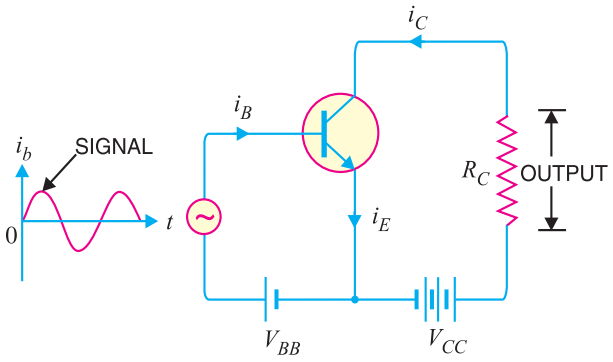


Fig. 8.33

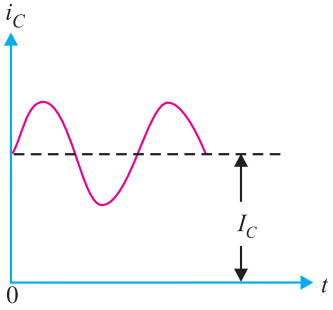


Fig. 8.34

Analysis of collector currents. When no signal is applied, the input circuit is forward biased by the battery V_{BB}. Therefore, a d.c. collector current I_C flows in the collector circuit. This is called *zero signal collector current*. When the signal voltage is applied, the forward bias on the emitter-base junction increases or decreases depending upon whether the signal is positive or negative. During the positive half-cycle of the signal, the forward bias on emitter-base junction is increased, causing total collector current i_C to increase. Reverse will happen for the negative half-cycle of the signal.

Fig. 8.34 shows the graph of total collector current i_C versus time. From the graph, it is clear that total collector current consists of two components, namely ;

(*i*) The d.c. collector current I_C (zero signal collector current) due to bias battery V_{BB}. This is the current that flows in the collector in the absence of signal.

(*ii*) The a.c. collector current i_c due to signal.

$\therefore$ Total collector current, $i_C = i_c + I_C$

The useful output is the voltage drop across collector load R_C due to the a.c. component i_c. The purpose of zero signal collector current is to ensure that the emitter-base junction is forward biased at all times. The table below gives the symbols usually employed for currents and voltages in transistor applications.

S. No.	Particular	Instantaneous a.c.	d.c.	Total
1.	Emitter current	i_e	I_E	i_E
2.	Collector current	i_c	I_C	i_C
3.	Base current	i_b	I_B	i_B
4.	Collector-emitter voltage	v_{ce}	V_{CE}	v_{CE}
5.	Emitter-base voltage	v_{eb}	V_{EB}	v_{EB}

8.17 Transistor Load Line Analysis

In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages. One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as *load line method* can be used to solve such problems. As explained later in this section, this method is quite easy and is frequently used in the analysis of transistor applications.

d.c. load line. Consider a common emitter *npn* transistor circuit shown in Fig. 8.35 (*i*) where no signal is applied. Therefore, d.c. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig. 8.35 (*ii*).

The value of collector-emitter voltage V_{CE} at any time is given by ;

$$V_{CE} = V_{CC} - I_C R_C \qquad ...(i)$$

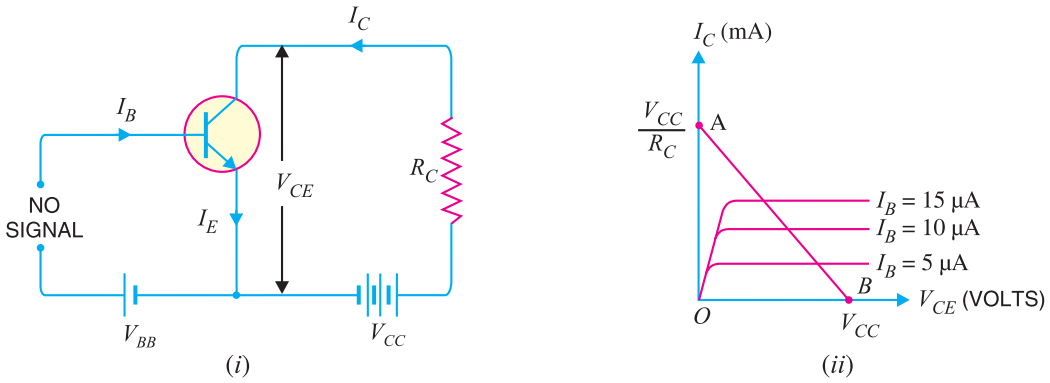


Fig. 8.35

As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as *d.c. load line* and determines the locus of $V_{CE} - I_C$ points for any given value of R_C. To add load line, we need two end points of the straight line. These two points can be located as under :

(*i*) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC} *i.e.*

$$\text{Max. } V_{CE} = V_{CC} - I_C R_C$$
$$= V_{CC} \qquad (\because I_C = 0)$$

This gives the first point B ($OB = V_{CC}$) on the collector-emitter voltage axis as shown in Fig. 8.35 (*ii*).

(*ii*) When collector-emitter voltage $V_{CE} = 0$, the collector current is maximum and is equal to V_{CC}/R_C *i.e.*

$$V_{CE} = V_{CC} - I_C R_C$$

or $$0 = V_{CC} - I_C R_C$$

$\therefore$ $$\text{Max. } I_C = V_{CC}/R_C$$

This gives the second point A ($OA = V_{CC}/R_C$) on the collector current axis as shown in Fig. 8.35 (*ii*). By joining these two points, d.c. *load line AB is constructed.

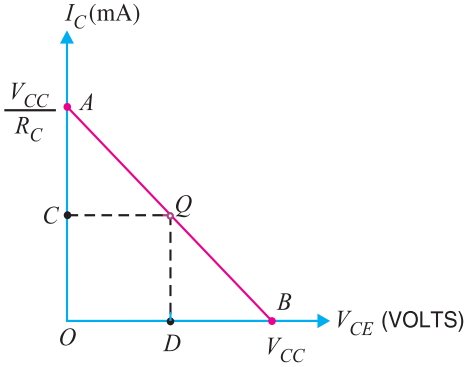


Fig. 8.36

Importance. The current (I_C) and voltage (V_{CE}) conditions in the transistor circuit are represented by some point on the output characteristics. The same information can be obtained from the load line. Thus when I_C is maximum ($= V_{CC}/R_C$), then $V_{CE} = 0$ as shown in Fig. 8.36. If $I_C = 0$, then V_{CE} is maximum

* **Why load line ?** The resistance R_C connected to the device is called load or load resistance for the circuit and, therefore, the line we have just constructed is called the load line.

and is equal to V_{CC}. For any other value of collector current say OC, the collector-emitter voltage $V_{CE} = OD$. It follows, therefore, that load line gives a far more convenient and direct solution to the problem.

Note. If we plot the load line on the output characteristic of the transistor, we can investigate the behaviour of the transistor amplifier. It is because we have the transistor output current and voltage specified in the form of load line equation and the transistor behaviour itself specified implicitly by the output characteristics.

8.18 Operating Point

The zero signal values of I_C and V_{CE} are known as the **operating point**.

It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also called quiescent (silent) point or *Q-point* because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent *i.e.* in the absence of the signal.

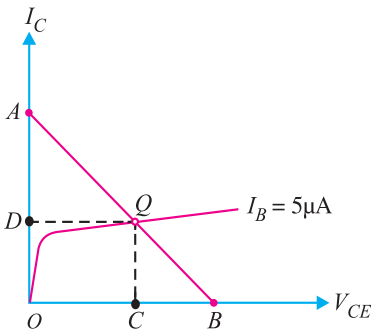


Fig. 8.37

Suppose in the absence of signal, the base current is 5 μA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on $I_B = 5$ μA characteristic. But I_C and V_{CE} conditions in the circuit should also be represented by some point on the d.c. load line AB. The point Q where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point Q describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point. Referring to Fig. 8.37, for $I_B = 5$ μA, the zero signal values are :

$$V_{CE} = OC \text{ volts}$$
$$I_C = OD \text{ mA}$$

It follows, therefore, that the zero signal values of I_C and V_{CE} (*i.e.* operating point) are determined by the point where d.c. load line intersects the proper base current curve.

Example 8.22. *For the circuit shown in Fig. 8.38 (i), draw the d.c. load line.*

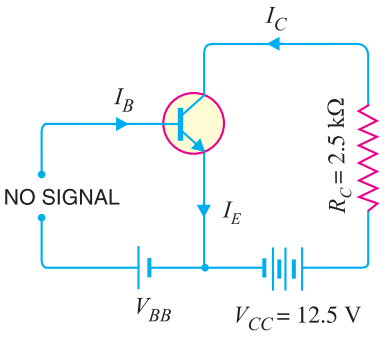
Solution. The collector-emitter voltage V_{CE} is given by ;

$$V_{CE} = V_{CC} - I_C R_C \qquad ...(i)$$

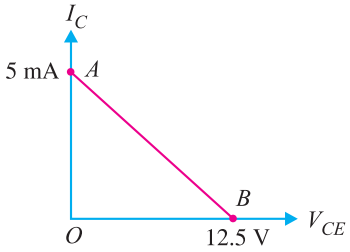
When $I_C = 0$, then,

$$V_{CE} = V_{CC} = 12.5 \text{ V}$$

This locates the point B of the load line on the collector-emitter voltage axis.



(*i*)



(*ii*)

Fig. 8.38

When $V_{CE} = 0$, then,

$I_C = V_{CC}/R_C = 12.5\ V/2.5\ k\Omega = 5\ mA$

This locates the point *A* of the load line on the collector current axis. By joining these two points, we get the d.c. load line *AB* as shown in Fig. 8.38 (*ii*).

Example 8.23. *In the circuit diagram shown in Fig. 8.39 (i), if $V_{CC} = 12V$ and $R_C = 6\ k\Omega$, draw the d.c. load line. What will be the Q point if zero signal base current is 20μA and $\beta = 50$?*

Solution. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 12$ V. This locates the point *B* of the load line. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 12\ V/6\ k\Omega = 2$ mA. This locates the point *A* of the load line. By joining these two points, load line *AB* is constructed as shown in Fig. 8.39 (*ii*).

Zero signal base current, $I_B = 20\ \mu A = 0.02$ mA

Current amplification factor, $\beta = 50$

$\therefore$ Zero signal collector current, $I_C = \beta I_B = 50 \times 0.02 = 1$ mA

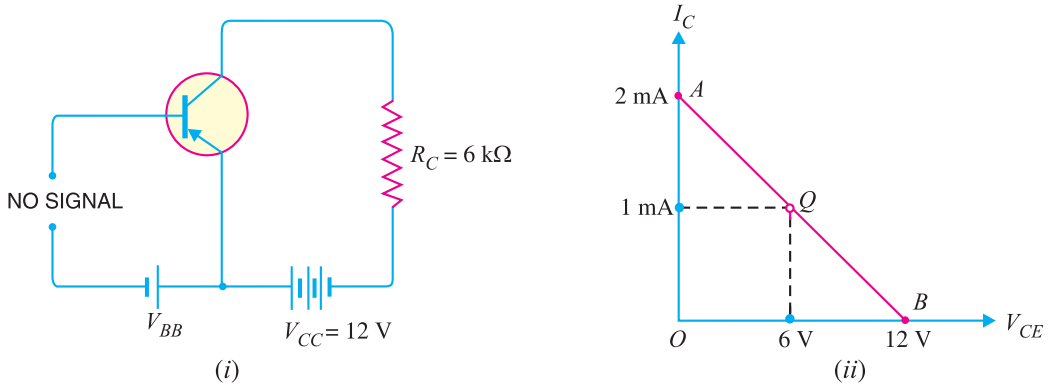


Fig. 8.39

Zero signal collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 12 - 1\ mA \times 6\ k\Omega = 6\ V$$

$\therefore$ Operating point is **6 V, 1 mA**.

Fig. 8.39 (*ii*) shows the *Q* point. Its co-ordinates are $I_C = 1$ mA and $V_{CE} = 6$ V.

Example 8.24. *In a transistor circuit, collector load is 4 kΩ whereas quiescent current (zero signal collector current) is 1mA.*

(i) What is the operating point if $V_{CC} = 10$ V ?

(ii) What will be the operating point if $R_C = 5\ k\Omega$?

Solution. $V_{CC} = 10$ V, $I_C = 1$ mA

(*i*) When collector load $R_C = 4\ k\Omega$, then,

$V_{CE} = V_{CC} - I_C R_C = 10 - 1\ mA \times 4\ k\Omega = 10 - 4 = 6\ V$

$\therefore$ Operating point is **6 V, 1 mA**.

(*ii*) When collector load $R_C = 5\ k\Omega$, then,

$V_{CE} = V_{CC} - I_C R_C = 10 - 1\ mA \times 5\ k\Omega = 10 - 5 = 5\ V$

$\therefore$ Operating point is **5 V, 1 mA**.

Example 8.25. *Determine the Q point of the transistor circuit shown in Fig. 8.40. Also draw the d.c. load line. Given $\beta = 200$ and $V_{BE} = 0.7V$.*

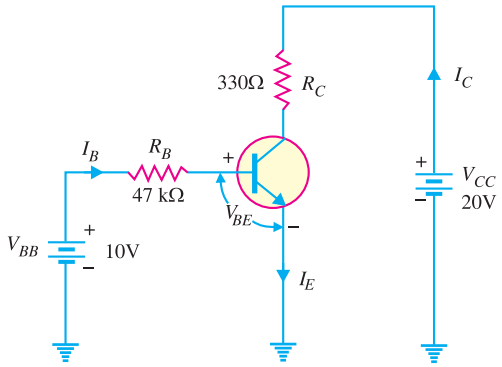


Fig 8.40

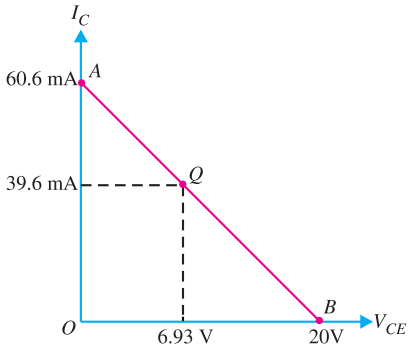


Fig. 8.41

Solution. The presence of resistor R_B in the base circuit should not disturb you because we can apply Kirchhoff's voltage law to find the value of I_B and hence I_C ($= \beta I_B$). Referring to Fig. 8.40 and applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{47\ k\Omega} = 198\ \mu A$$

Now $I_C = \beta I_B = (200)(198\ \mu A) = 39.6\ mA$

Also $V_{CE} = V_{CC} - I_C R_C = 20V - (39.6mA)\ (330\ \Omega) = 20V - 13.07V = 6.93V$

Therefore, the Q-point is $I_C =$ **39.6 mA** and $V_{CE} =$ **6.93V.**

D.C. load line. In order to draw the d.c. load line, we need two end points.

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 20V$. This locates the point B of the load line on the collector-emitter voltage axis as shown in Fig. 8.41. When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 20V/330\Omega = 60.6$ mA. This locates the point A of the load line on the collector current axis. By joining these two points, d.c. load line AB is constructed as shown in Fig. 8.41.

Example 8.26. *Determine the Q point of the transistor circuit shown in* *Fig. 8.42. *Also draw the d.c. load line. Given $\beta = 100$ and $V_{BE} = 0.7V$.*

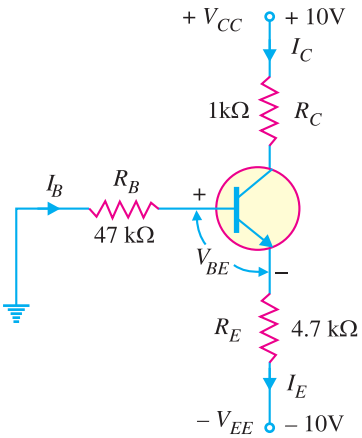


Fig. 8.42

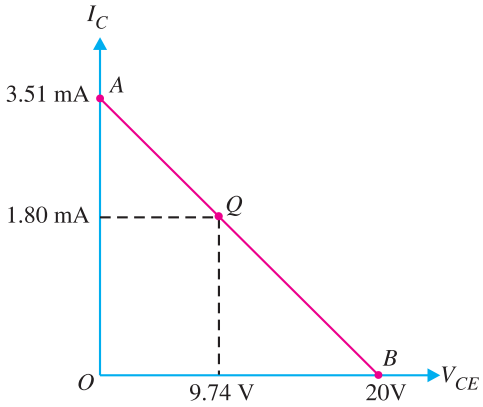


Fig. 8.43

* The presence of two power supplies has an effect on the baisc equations for I_C and V_{CE} used for single power supply (*i.e.* V_{CC}). Normally, the two supply voltages will be equal. For example, if $V_{CC} = +10V$ (d.c.), then $V_{EE} = -10$ V (d.c.).

Solution. The transistor circuit shown in Fig. 8.42 may look complex but we can easily apply Kirchhoff's voltage law to find the various voltages and currents in the * circuit.

Applying Kirchhoff's voltage law to the base-emitter loop, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0 \quad \text{or} \quad V_{EE} = I_B R_B + I_E R_E + V_{BE}$$

Now $I_C = \beta I_B$ and $I_C \simeq I_E$. $\therefore \; I_B = I_E/\beta$. Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or
$$I_E \left(\frac{R_B}{\beta} + R_E\right) = V_{EE} - V_{BE} \quad \text{or} \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$,
$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{10\text{V} - 0.7\text{V}}{4.7\ \text{k}\Omega + 47\ \text{k}\Omega/100} = \frac{9.3\ \text{V}}{5.17\ \text{k}\Omega} = 1.8\ \text{mA}$$

Applying Kirchhoff's voltage law to the collector side, we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

or
$$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E) \qquad (\text{Q} \quad I_E \simeq I_C)$$
$$= 10\text{V} + 10\text{V} - 1.8\ \text{mA}\ (1\ \text{k}\Omega + 4.7\ \text{k}\Omega) = 9.74\text{V}$$

Therefore, the operating point of the circuit is $I_C = \mathbf{1.8\ mA}$ and $V_{CE} = \mathbf{9.74V}$.

D.C. load line. The d.c. load line can be constructed as under :

$$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

When $I_C = 0$; $V_{CE} = V_{CC} + V_{EE} = 10\text{V} + 10\text{V} = 20\text{V}$. This locates the first point B ($OB = 20\text{V}$) of the load line on the collector-emitter voltage axis. When $V_{CE} = 0$,

$$I_C = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{10V + 10V}{1\ k\Omega + 4.7\ k\Omega} = \frac{20V}{5.7\ k\Omega} = 3.51\ \text{mA}$$

This locates the second point A ($OA = 3.51$ mA) of the load line on the collector current axis. By joining points A and B, d.c. load line AB is constructed as shown in Fig. 8.43.

Example 8.27. *In the above example, find (i) emitter voltage w.r.t. ground (ii) base voltage w.r.t. ground (iii) collector voltage w.r.t. ground.*

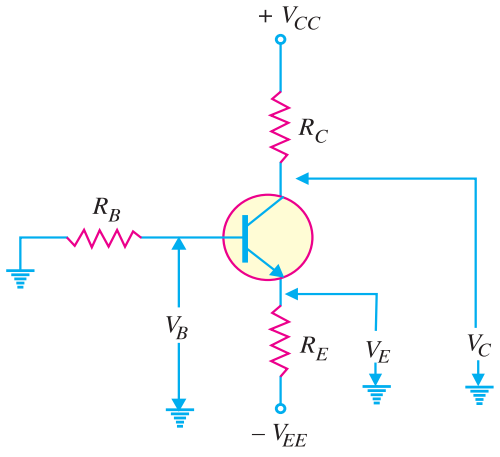


Fig. 8.44

* The emitter resistor R_E provides stabilisation of Q-point (See Art. 9.12).

Solution. Refer to Fig. 8.44.

(*i*) The emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E = -10\text{V} + 1.8\text{ mA} \times 4.7\text{ k}\Omega = \mathbf{-1.54V}$$

(*ii*) The base voltage w.r.t. ground is

$$V_B = V_E + V_{BE} = 10\text{V} + 0.7\text{V} = \mathbf{10.7V}$$

(*iii*) The collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C = 10\text{V} - 1.8\text{ mA} \times 1\text{ k}\Omega = \mathbf{8.2V}$$

8.19 Practical Way of Drawing CE Circuit

The common emitter circuits drawn so far can be shown in another convenient way. Fig. 8.45 shows the practical way of drawing *CE* circuit. In Fig. 8.45 (*i*), the practical way of drawing common emitter *npn* circuit is shown. Similarly, Fig. 8.45 (*ii*) shows the practical way of drawing common emitter *pnp* circuit. In our further discussion, we shall often use this scheme of presentation.

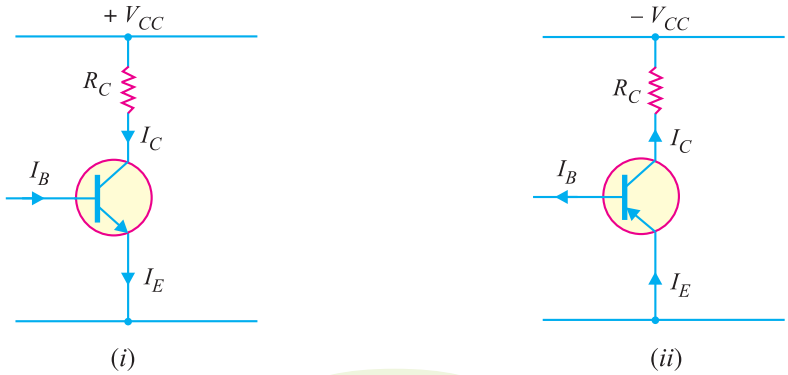


Fig. 8.45

8.20 Output from Transistor Amplifier

A transistor raises the strength of a weak signal and thus acts as an amplifier. Fig. 8.46 shows the common emitter amplifier. There are two ways of taking output from this transistor connection. The output can be taken either across R_C or across terminals 1 and 2. In either case, the magnitude of output is the same. This is clear from the following discussion :

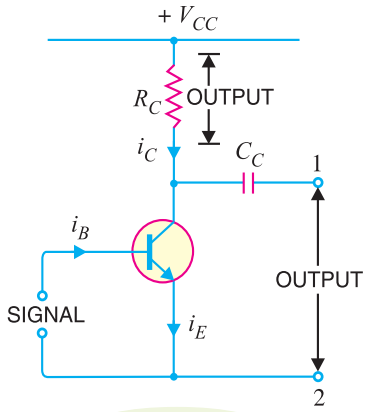


Fig. 8.46

(*i*) First method. We can take the output directly by putting a load resistance R_C in the collector circuit *i.e.*

$$\text{Output} = \text{voltage across } R_C = i_c R_C \qquad ...(i)$$

This method of taking output from collector load is used only in single stage of amplification.

(*ii*) Second method. The output can also be taken across terminals 1 and 2 *i.e.* from collector and emitter end of supply.

$$\text{Output} = \text{Voltage across terminals 1 and 2}$$
$$= V_{CC} - i_c R_C$$

As V_{CC} is a direct voltage and cannot pass through capacitor C_C, therefore, only varying voltage $i_c R_C$ will appear across terminals 1 and 2.

$$\therefore \qquad \text{Output} = -i_c R_C \qquad ...(ii)$$

From exps. (*i*) and (*ii*), it is clear that magnitude of output is the same whether we take output across collector load or terminals 1 and 2. The minus sign in exp. (*ii*) simply indicates the phase reversal. The second method of taking output is used in multistages of amplification.

8.21 Performance of Transistor Amplifier

The performance of a transistor amplifier depends upon input resistance, output resistance, effective collector load, current gain, voltage gain and power gain. As *common emitter connection* is universally adopted, therefore, we shall explain these terms with reference to this mode of connection.

(*i*) Input resistance. *It is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage i.e.*

$$\text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

The value of input resistance is quite small because the input circuit is always forward biased. It ranges from 500 Ω for small low powered transistors to as low as 5 Ω for high powered transistors. In fact, input resistance is the opposition offered by the base-emitter junction to the signal flow. Fig. 8.47 shows the general form of an amplifier. The input voltage V_{BE} causes an input current I_B.

$$\therefore \quad \text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{V_{BE}}{I_B}$$

Thus if the input resistance of an amplifier is 500 Ω and the signal voltage at any instant is 1 V, then,

$$\text{Base current, } i_b = \frac{1\,V}{500\,\Omega} = 2\text{ mA}$$

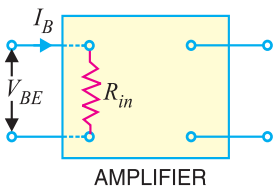


Fig. 8.47

(*ii*) Output resistance. *It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current i.e.*

$$\text{Output resistance, } R_O = \frac{\Delta V_{CE}}{\Delta I_C}$$

The output characteristics reveal that collector current changes very slightly with the change in collector-emitter voltage. Therefore, output resistance of a transistor amplifier is very high– of the order of several hundred kilo-ohms. The physical explanation of high output resistance is that collector-base junction is reverse biased.

(*iii*) Effective collector load. *It is the total load as seen by the a.c. collector current.*

In case of single stage amplifiers, the effective collector load is a parallel combination of R_C and R_O as shown in Fig. 8.48 (*i*).

$$\text{Effective collector load, } R_{AC} = R_C \parallel R_O$$
$$= \frac{R_C \times R_O}{R_C + R_O} = {}^*R_C$$

It follows, therefore, that for a single stage amplifier, effective load is equal to collector load R_C.

However, in a multistage amplifier (*i.e.* having more than one amplification stage), the input resistance R_i of the next stage also comes into picture as shown in Fig. 8.48 (*ii*). Therefore, effective collector load becomes parallel combination of R_C, R_O and R_i *i.e.*

$$\text{Effective collector load, } R_{AC} = R_C \parallel R_O \parallel R_i$$

* As output resistance R_O is several times R_C, therefore, R_C can be neglected as compared to R_O.

$$R_{AC} = \frac{R_C \times R_O}{R_O} = R_C$$

$$= {}^{*}R_C \,||\, R_i = \frac{R_C\, R_i}{R_C + R_i}$$

As input resistance R_i is quite small (25 Ω to 500 Ω), therefore, effective load is reduced.

(iv) Current gain. *It is the ratio of change in collector current* (ΔI_C) *to the change in base current* (ΔI_B) *i.e.*

$$\text{Current gain, } \beta = \frac{\Delta I_C}{\Delta I_B}$$

The value of β ranges from 20 to 500. The current gain indicates that input current becomes β times in the collector circuit.

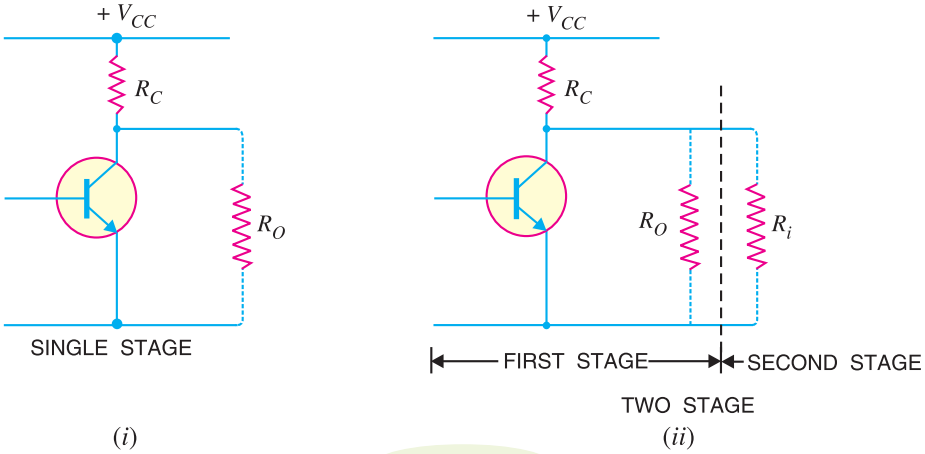


Fig. 8.48

(v) Voltage gain. *It is the ratio of change in output voltage* (ΔV_{CE}) *to the change in input voltage* (ΔV_{BE}) *i.e.*

$$\text{Voltage gain, } A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

$$= \frac{\text{Change in output current} \times \text{effective load}}{\text{Change in input current} \times \text{input resistance}}$$

$$= \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i} = \frac{\Delta I_C}{\Delta I_B} \times \frac{R_{AC}}{R_i} = \beta \times \frac{R_{AC}}{R_i}$$

For single stage, $R_{AC} = R_C$. However, for multistage, $R_{AC} = \dfrac{R_C \times R_i}{R_C + R_i}$ where R_i is the input resistance of the next stage.

(vi) Power gain. *It is the ratio of output signal power to the input signal power i.e.*

$$\text{Power gain, } A_p = \frac{(\Delta I_C)^2 \times R_{AC}}{(\Delta I_B)^2 \times R_i} = \left(\frac{\Delta I_C}{\Delta I_B}\right) \times \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i}$$

$$= \text{Current gain} \times \text{Voltage gain}$$

Example 8.28. *A change of 200 mV in base-emitter voltage causes a change of 100 μA in the base current. Find the input resistance of the transistor.*

Solution. Change in base-emitter voltage is

* $R_C \,||\, R_O = R_C$ as already explained.

$\Delta V_{BE} = 200$ mV

Change in base current, $\Delta I_B = 100\ \mu A$

$\therefore$ Input resistance, $R_i = \dfrac{\Delta V_{BE}}{\Delta I_B} = \dfrac{200\text{ mV}}{100\ \mu\text{ A}} = \mathbf{2\ k\Omega}$

Example 8.29. *If the collector current changes from 2 mA to 3mA in a transistor when collector-emitter voltage is increased from 2V to 10V, what is the output resistance ?*

Solution. Change in collector-emitter voltage is

$\Delta V_{CE} = 10 - 2 = 8$ V

Change in collector current is $\Delta I_C = 3 - 2 = 1$ mA

$\therefore$ Output resistance, $R_O = \dfrac{\Delta V_{CE}}{\Delta I_C} = \dfrac{8\text{ V}}{1\text{ mA}} = \mathbf{8\ k\Omega}$

Example 8.30. *For a single stage transistor amplifier, the collector load is $R_C = 2k\Omega$ and the input resistance $R_i = 1k\Omega$. If the current gain is 50, calculate the voltage gain of the amplifier.*

Solution. Collector load, $R_C = 2\ k\Omega$

Input resistance, $R_i = 1\ k\Omega$

Current gain, $\beta = 50$

$\therefore$ Voltage gain, $A_v = \beta \times \dfrac{R_{AC}}{R_i} = \beta \times \dfrac{R_C}{R_i}$ [$\because$ For single stage, $R_{AC} = R_C$]

$= 50 \times (2/1) = \mathbf{100}$

8.22 Cut off and Saturation Points

Fig. 8.49 (*i*) shows *CE* transistor circuit while Fig. 8.49 (*ii*) shows the output characteristcs along with the d.c. load line.

(*i*) Cut off. The point where the load line intersects the $I_B = 0$ curve is known as *cut off*. At this point, $I_B = 0$ and only small collector current (*i.e.* collector leakage current I_{CEO}) exists. At cut off, the base-emitter junction no longer remains forward biased and normal transistor action is lost. The collector-emitter voltage is nearly equal to V_{CC} *i.e.*

$$V_{CE\ (cut\ off)} = V_{CC}$$

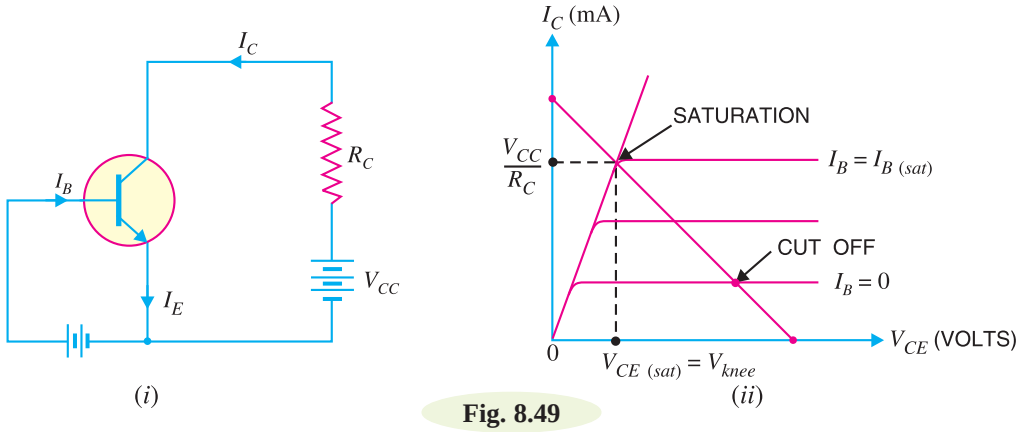


Fig. 8.49

(*ii*) Saturation. The point where the load line intersects the $I_B = I_{B(sat)}$ curve is called *saturation*. At this point, the base current is maximum and so is the collector current. At saturation, collector-base junction no longer remains reverse biased and normal transistor action is lost.

$$I_{C\,(sat)} \simeq \frac{V_{CC}}{R_C}; \quad V_{CE} = V_{CE(sat)} = V_{knee}$$

If base current is greater than $I_{B(sat)}$, then collector current cannot increase because collector-base junction is no longer reverse-biased.

(*iii*) Active region. The region between cut off and saturation is known as *active region*. In the active region, collector-base junction remains reverse biased while base-emitter junction remains forward biased. Consequently, the transistor will function normally in this region.

Note. We provide biasing to the transistor to ensure that it operates in the active region. The reader may find the detailed discussion on transistor biasing in the next chapter.

Summary. A transistor has two *pn* junctions *i.e.*, it is like two diodes. The junction between base and emitter may be called *emitter diode*. The junction between base and collector may be called *collector diode*. We have seen above that transistor can act in one of the three states : **cut-off, saturated** and **active**. The state of a transistor is entirely determined by the states of the emitter diode and collector diode [See Fig. 8.50]. The relations between the diode states and the transistor states are :

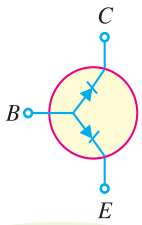


Fig. 8.50

CUT-OFF : Emitter diode and collector diode are **OFF.**

ACTIVE : Emitter diode is **ON** and collector diode is **OFF.**

SATURATED : Emitter diode and collector diode are **ON.**

In the **active state**, collector current [See Fig 8.51 (*i*)] is β times the base current (*i.e.* $I_C = \beta I_B$). If the transistor is **cut-off,** there is no base current, so there is no collector or emitter current. That is collector emitter pathway is open [See Fig. 8.51 (*ii*)]. In **saturation**, the collector and emitter are, in effect, shorted together. That is the transistor behaves as though a switch has been closed between the collector and emitter [See Fig. 8.51 (*iii*)].

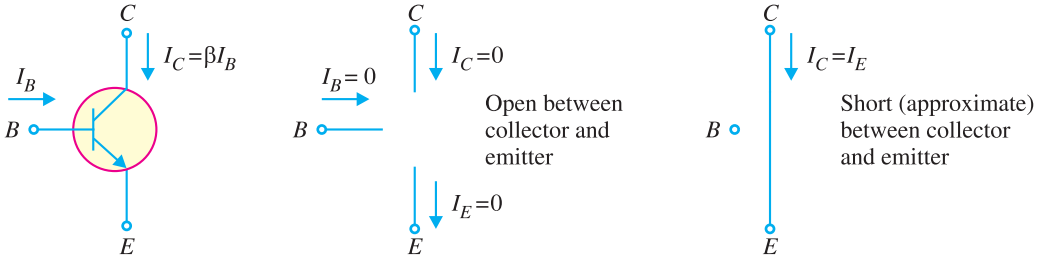


Fig. 8.51

Note. When the transistor is in the active state, $I_C = \beta I_B$. Therefore, a transistor acts as an amplifier when operating in the active state. Amplification means *linear amplification*. In fact, small signal amplifiers are the most common *linear devices*.

Example 8.31. *Find $I_{C(sat)}$ and $V_{CE(cut\ off)}$ for the circuit shown in Fig. 8.52 (i).*

Solution. As we decrease R_B, base current and hence collector current increases. The increased collector current causes a greater voltage drop across R_C; this decreases the collector-emitter voltage. Eventually at some value of R_B, V_{CE} decreases to V_{knee}. At this point, collector-base junction is no longer reverse biased and transistor action is lost. Consequently, further increase in collector current is not possible. The transistor conducts maximum collector current ; we say the transistor is saturated.

$$I_{C(sat)} = \frac{V_{CC} - {}^{*}V_{knee}}{R_C} = \frac{V_{CC}}{R_C} = \frac{20\,V}{1\,k\Omega} = \mathbf{20mA}$$

* V_{knee} is about 0.5 V for Ge transistor and about 1V for Si transistor. Consequently, V_{knee} can be neglected as compared to V_{CC} (= 20 V in this case).

As we increase R_B, base current and hence collector current decreases. This decreases the voltage drop across R_C. This increases the collector-emitter voltage. Eventually, when $I_B = 0$, the emitter-base junction is no longer forward biased and transistor action is lost. Consequently, further increase in V_{CE} is not possible. In fact, V_{CE} now equals to V_{CC}.

$$V_{CE(cut\text{-}off)} = V_{CC} = \mathbf{20\ V}$$

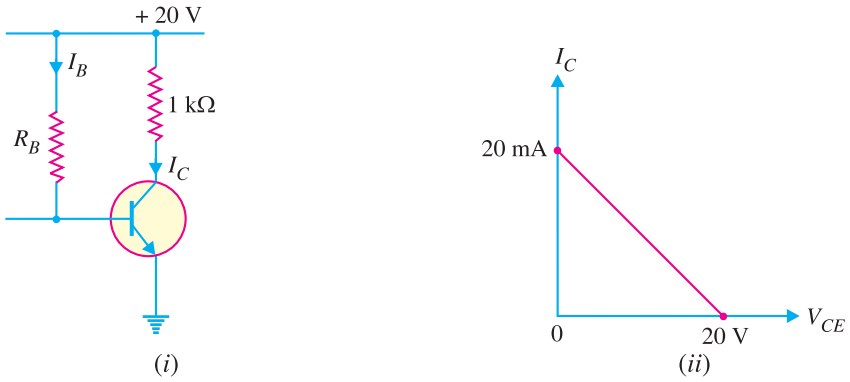


Fig. 8.52

Figure 8.52 (*ii*) shows the saturation and cut off points. Incidentally, they are end points of the d.c. load line.

Note. The exact value of $V_{CE(cut\text{-}off)} = V_{CC} - I_{CEO} R_C$. Since the collector leakage current I_{CEO} is very small, we can neglect $I_{CEO} R_C$ as compared to V_{CC}.

Example 8.32. *Determine the values of $V_{CE\ (off)}$ and $I_{C\ (sat)}$ for the circuit shown in Fig. 8.53.*

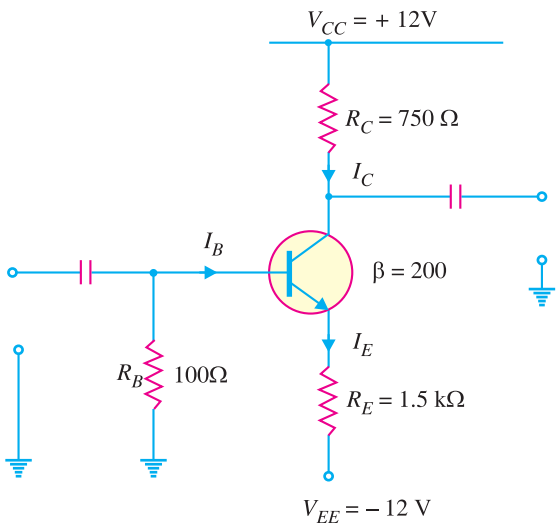


Fig. 8.53

Solution. Applying Kirchhoff's voltage law to the collector side of the circuit in Fig. 8.53, we have,

$$V_{CC} - I_C R_C - V_{CE} - {}^*I_C R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E) \quad \ldots (i)$$

* Voltage across $R_E = I_E R_E$. Since $I_E \simeq I_C$, voltage across $R_E = I_C R_E$.

We have $V_{CE\,(off)}$ when $I_C = 0$. Therefore, putting $I_C = 0$ in eq. (*i*), we have,

$$V_{CE\,(off)} = V_{CC} + V_{EE} = 12 + 12 = \mathbf{24V}$$

We have $I_{C\,(sat)}$ when $V_{CE} = 0$.

$$\therefore \quad I_{C\,(sat)} = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{(12+12)\,V}{(750+1500)\,\Omega} = \mathbf{10.67\ mA}$$

Example 8.33. *Determine whether or not the transistor in Fig. 8.54 is in stauration. Assume* $V_{knee} = 0.2V$.

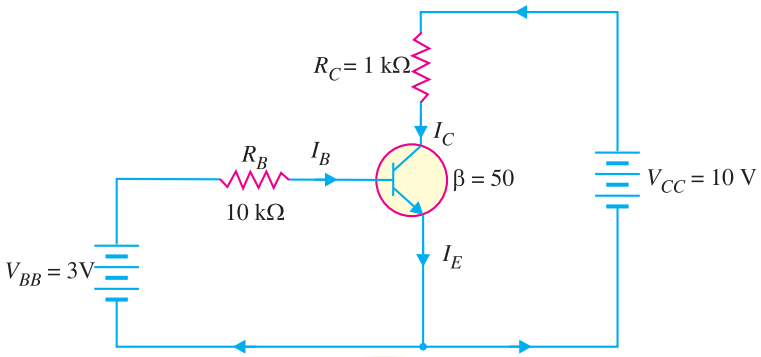


Fig. 8.54

Solution.

$$I_{C\,(sat)} = \frac{V_{CC} - V_{knee}}{R_C} = \frac{10\,V - 0.2\,V}{1\,k\Omega} = \frac{9.8\,V}{1\,k\Omega} = 9.8\ \text{mA}$$

Now we shall see if I_B is large enough to produce $I_{C\,(sat)}$.

$$\text{Now} \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3V - 0.7V}{10\,k\Omega} = \frac{2.3\,V}{10\,k\Omega} = 0.23\ \text{mA}$$

$$\therefore \quad I_C = \beta I_B = 50 \times 0.23 = 11.5\ \text{mA}$$

This shows that with specified β, this base current (= 0.23 mA) is capable of producing I_C greater than $I_{C\,(sat)}$. Therefore, the transistor is **saturated.** In fact, the collector current value of 11. 5 mA is never reached. If the base current value corresponding to $I_{C\,(sat)}$ is increased, the collector current remains at the saturated value (= 9.8 mA).

Example 8.34. *Is the transistor in Fig. 8.55 operating in saturated state ?*

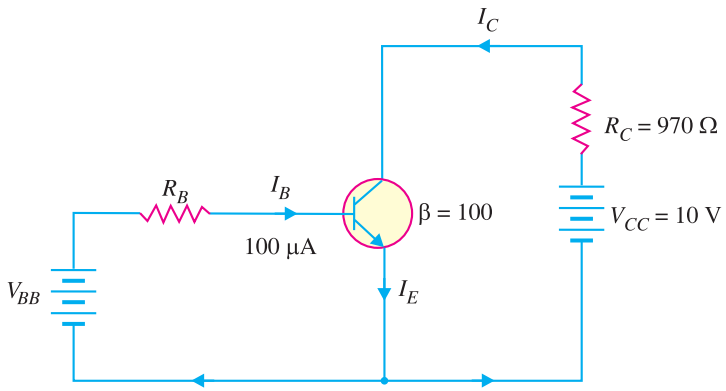


Fig. 8.55

Solution.

$$I_C = \beta I_B = (100)(100\ \mu A) = 10\ mA$$
$$V_{CE} = V_{CC} - I_C R_C$$
$$= 10V - (10\ mA)(970\Omega) = 0.3V$$

Let us relate the values found to the transistor shown in Fig. 8.56. As you can see, the value of V_{BE} is 0.95V and the value of $V_{CE} = 0.3V$. This leaves V_{CB} of 0.65V (Note that $V_{CE} = V_{CB} + V_{BE}$). In this case, collector – base junction (*i.e.*, collector diode) is forward biased as is the emitter-base junction (*i.e.*, emitter diode). Therefore, the transistor is operating in the **saturation region.**

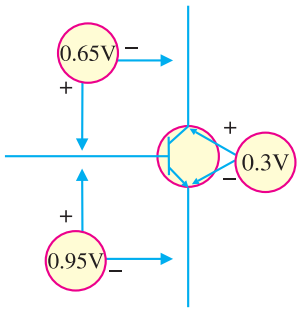


Fig. 8.56

Note. When the transistor is in the saturated state, the base current and collector current are independent of each other. The base current is still (and always is) found only from the base circuit. The collector current is found apporximately by closing the imaginary switch between the collector and the emitter in the collector circuit.

Example 8.35. *For the circuit in Fig. 8.57, find the base supply voltage (V_{BB}) that just puts the transistor into saturation. Assume $\beta = 200$.*

Solution. When transistor first goes into saturation, we can assume that the collector shorts to the emitter (*i.e.* $V_{CE} = 0$) but the collector current is still β times the base current.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - 0}{R_C}$$
$$= \frac{10V - 0}{2\ k\Omega} = 5\ mA$$

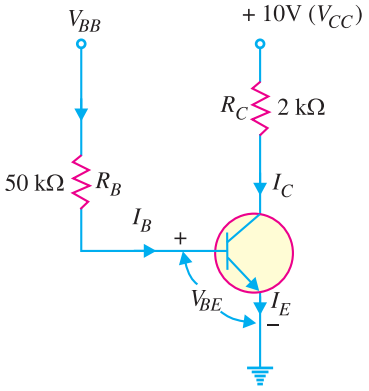


Fig. 8.57

The base current I_B corresponding to $I_{C\,(sat)}$ (=5 mA) is

$$I_B = \frac{I_{C\,(sat)}}{\beta} = \frac{5\ mA}{200} = 0.025\ mA$$

Applying Kirchhoff's voltage law to the base circuit, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or
$$V_{BB} = V_{BE} + I_B R_B$$
$$= 0.7V + 0.025\ mA \times 50\ k\Omega = 0.7 + 1.25 = 1.95V$$

Therefore, for $V_{BB} \geq 1.95$, the transistor will be in *saturation.*

Example. 8.36. *Determine the state of the transistor in Fig. 8.58 for the following values of collector resistor* :

(i) $R_C = 2\ k\Omega$ *(ii)* $R_C = 4\ k\Omega$ *(iii)* $R_C = 8\ k\Omega$

Solution. Since I_E does not depend on the value of the collector resistor R_C, the emitter current (I_E) is the same for all three parts.

Emitter voltage, $V_E = V_B - V_{BE} = V_{BB} - V_{BE}$
$= 2.7V - 0.7\ V = 2V$

Also
$$I_E = \frac{V_E}{R_E} = \frac{2V}{1\ k\Omega} = 2\ mA$$

(*i*) When $R_C = 2\ k\Omega$. Suppose the transistor is active.

$\therefore$ $I_C = I_E = 2\ mA$

$\therefore$ $I_B = I_C/\beta = 2\ mA/100 = 0.02\ mA$

Collector voltage, $V_C = V_{CC} - I_C R_C$
$= 10V - 2\ mA \times 2\ k\Omega = 10V - 4V = 6V$

Since V_C (= 6V) is greater than V_E (= 2V), the transistor is **active.** Therefore, our assumption that transistor is active is correct.

(ii) When R_C = 4 kΩ. Suppose the transistor is active.

$\therefore \quad I_C = 2mA$ and $I_B = 0.02$ mA ... as found above
Collector voltage, $V_C = V_{CC} - I_C R_C$
$= 10V - 2\ mA \times 4\ k\Omega = 10V - 8V = 2V$

Since $V_C = V_E$, the transistor is just at the edge of **saturation.** We know that at the edge of saturation, the relation between the transistor currents is the same as in the **active state.** Both answers are correct.

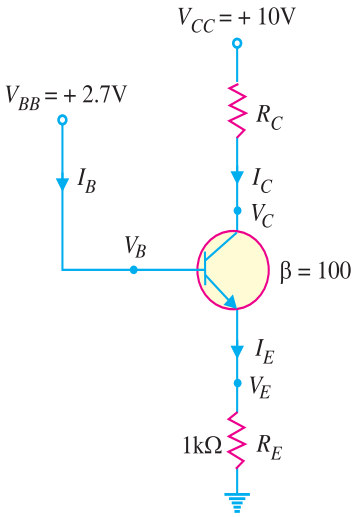


Fig. 8.58

(iii) When R_C = 8 kΩ. Suppose the transistor is active.

$\therefore \quad I_C = 2mA$; $I_B = 0.02$ mA ... as found earlier.
Collector voltage, $V_C = V_{CC} - I_C R_C$
$= 10V - 2\ mA \times 8\ k\Omega = 10V - 16V = -6V$

Since $V_C < V_E$, the transistor is **saturated** and our assumption is not correct.

Example 8.37. *In the circuit shown in Fig. 8.59, V_{BB} is set equal to the following values : (i) V_{BB} = 0.5V (ii) V_{BB} = 1.5V (iii) V_{BB} = 3V*
Determine the state of the transistor for each value of the base supply voltage V_{BB}.

Solution. The state of the transistor also depends on the base supply voltage V_{BB}.

(i) For V_{BB} = 0.5V

Because the base voltage V_B (= V_{BB} = 0.5V) is less than 0.7V, the transistor is **cut-off.**

(ii) For V_{BB} = 1.5V

The base voltage V_B controls the emitter voltage V_E which controls the emitter current I_E.

Now $\quad V_E = V_B - 0.7V = 1.5V - 0.7V = 0.8V$

$\therefore \quad I_E = \dfrac{V_E}{R_E} = \dfrac{0.8\,V}{1\,k\Omega} = 0.8$ mA

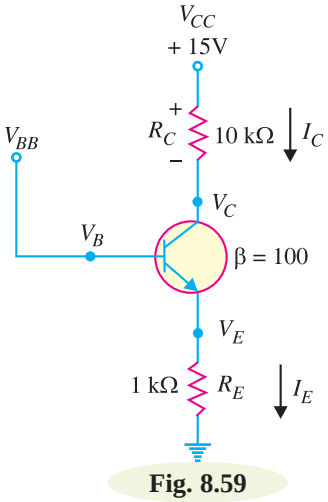


Fig. 8.59

If the transistor is active, we have,

$I_C = I_E = 0.8$ mA and $I_B = I_C/\beta = 0.8/100 = 0.008$ mA

$\therefore$ Collector voltage, $V_C = V_{CC} - I_C R_C$
$= 15V - 0.8\ mA \times 10\ k\Omega = 15V - 8V = 7V$

Since $V_C > V_E$, the transistor is **active** and our assumption is correct.

(iii) For V_{BB} = 3V

$V_E = V_B - 0.7V = 3V - 0.7V = 2.3V$

$\therefore \quad I_E = \dfrac{V_E}{R_E} = \dfrac{2.3\,V}{1\,k\Omega} = 2.3$ mA

Assuming the transistor is active, we have,

$$I_C = I_E = 2.3 \text{ mA} \quad ; \quad I_B = I_C/\beta = 2.3/100 = 0.023 \text{ mA}$$

Collector voltage, $V_C = V_{CC} - I_C R_C$

$= 15\text{V} - 2.3 \text{ mA} \times 10 \text{ k}\Omega = 15\text{V} - 23\text{V} = -8\text{V}$

Since $V_C < V_E$, the transistor is **saturated** and our assumption is not correct.

8.23 Power Rating of Transistor

The maximum power that a transistor can handle without destruction is known as **power rating** *of the transistor*.

When a transistor is in operation, almost all the power is dissipated at the reverse biased *collector-base junction. The power rating (or maximum power dissipation) is given by :

$$P_{D\ (max)} = \text{Collector current} \times \text{Collector-base voltage}$$

$$= I_C \times V_{CB}$$

$$\therefore \quad P_{D\ (max)} = I_C \times V_{CE}$$

$[\because V_{CE} = V_{CB} + V_{BE}$. Since V_{BE} is very small, $V_{CB} \simeq V_{CE}]$

While connecting transistor in a circuit, it should be ensured that its power rating is not exceeded otherwise the transistor may be destroyed due to excessive heat. For example, suppose the power rating (or maximum power dissipation) of a transistor is 300 mW. If the collector current is 30 mA, then maximum V_{CE} allowed is given by ;

$$P_{D\ (max)} = I_C \times V_{CE\ (max)}$$

or $$300 \text{ mW} = 30 \text{ mA} \times V_{CE\ (max)}$$

or $$V_{CE\ (max)} = \frac{300 \text{ mW}}{30 \text{ mA}} = 10\text{V}$$

This means that for $I_C = 30$ mA, the maximum V_{CE} allowed is 10V. If V_{CE} exceeds this value, the transistor will be destroyed due to excessive heat.

Maximum power dissipation curve. For **power transistors, it is sometimes necessary to draw maximum power dissipation curve on the output characteristics. To draw this curve, we should know the power rating (*i.e.* maximum power dissipation) of the transistor. Suppose the power rating of a transistor is 30 mW.

$$P_{D\ (max)} = V_{CE} \times I_C$$

or $$30 \text{ mW} = V_{CE} \times I_C$$

Using convenient V_{CE} values, the corresponding collector currents are calculated for the maximum power dissipation. For example, for $V_{CE} = 10$V,

$$I_C\ (max) = \frac{P_{D\ (max)}}{V_{CE}} = \frac{30 \text{ mW}}{10 \text{ V}} = 3\text{mA}$$

This locates the point *A* (10V, 3 mA) on the output characteristics. Similarly, many points such as *B, C, D etc.* can be located on the output characteristics. Now draw a curve through the above points to obtain the maximum power dissipation curve as shown in Fig. 8.60.

In order that transistor may not be destroyed, the transistor voltage and current (*i.e.* V_{CE} and I_C) conditions must at all times be maintained in the portion of the characteristics below the maximum power dissipation curve.

* The base-emitter junction conducts about the same current as the collector-base junction (*i.e.* $I_E \simeq I_C$). However, V_{BE} is very small (0.3 V for *Ge* transistor and 0.7 V for *Si* transistor). For this reason, power dissipated at the base-emitter junction is negligible.

** A transistor that is suitable for large power amplification is called a *power transistor*. It differs from other transistors mostly in size ; it is considerably larger to provide for handling the great amount of power.

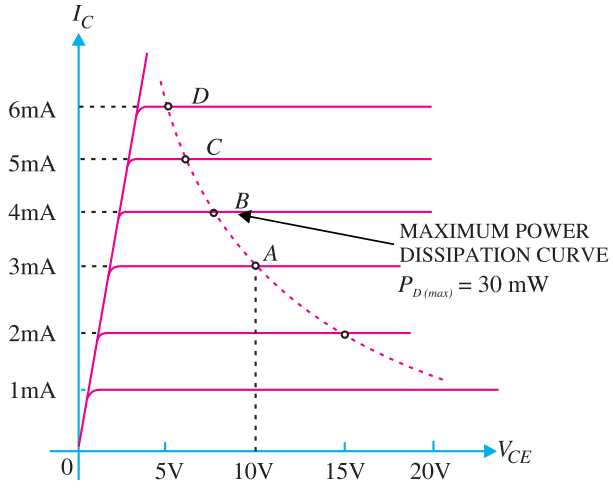


Fig. 8.60

Example 8.38. *The maximum power dissipation of a transistor is 100mW. If V_{CE} = 20V, what is the maximum collector current that can be allowed without destruction of the transistor?*

Solution.

$$P_{D\,(max)} = V_{CE} \times I_{C\,(max)}$$

or $$100 \text{ mW} = 20 \text{ V} \times I_{C\,(max)}$$

$$\therefore \quad I_{C\,(max)} = \frac{100 \text{ mW}}{20 \text{ V}} = \mathbf{5 \text{ mA}}$$

Thus for V_{CE} = 20V, the maximum collector current allowed is 5 mA. If collector current exceeds this value, the transistor may be burnt due to excessive heat.

Note. Suppose the collector current becomes 7mA. The power produced will be 20 V × 7 mA = 140 mW. The transistor can only dissipate 100 mW. The remaining 40 mW will raise the temperature of the transistor and eventually it will be burnt due to excessive heat.

Example 8.39. *For the circuit shown in Fig. 8.61, find the transistor power dissipation. Assume that β = 200.*

Solution.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{(5 - 0.7)\,V}{1\,k\Omega} = 4.3 \text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 200 \times 4.3 = 860 \text{ mA}$$

Now $$V_{CE} = V_{CC} - I_C R_C = 5 - I_C \times 0 = 5\text{V}$$

$\therefore$ Power dissipation, $P_D = V_{CE} \times I_C$

$$= 5\text{V} \times 860 \text{ mA} = 4300 \text{ mW} = \mathbf{4.3W}$$

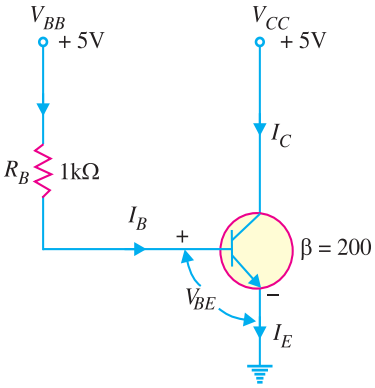


Fig. 8.61

Example 8.40. *For the circuit shown in Fig. 8.62, find the power dissipated in the transistor. Assume β = 100.*

Solution. The transistor is usually used with a resistor R_C connected between the collector and its power supply V_{CC} as shown is Fig. 8.62. The collector resistor R_C serves two purposes. Firstly, it allows us to control the voltage V_C at the collector. Secondly, it protects the transistor from excessive collector current I_C and, therefore, from excessive power dissipation.

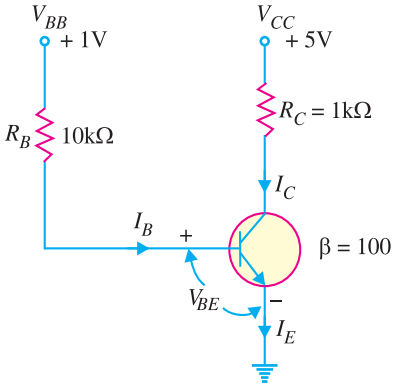


Fig. 8.62

Referring to Fig. 8.62 and applying Kirchhoff's voltage law to the base side, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{1V - 0.7V}{10\,k\Omega} = \frac{0.3V}{10\,k\Omega} = 0.03 \text{ mA}$$

Now $I_C = \beta I_B = 100 \times 0.03 = 3$ mA

$\therefore \quad V_{CE} = V_{CC} - I_C R_C = 5\text{V} - 3 \text{ mA} \times 1 \text{ k}\Omega = 5\text{V} - 3\text{V} = 2\text{V}$

$\therefore$ Power dissipated in the transistor is

$$P_D = V_{CE} \times I_C = 2\text{V} \times 3 \text{ mA} = \mathbf{6 \text{ mW}}$$

Example 8.41. *The transistor in Fig. 8.63 has the following maximum ratings :*

$$P_{D\,(max)} = 800 \text{ mW} ; V_{CE\,(max)} = 15\text{V} ; I_{C\,(max)} = 100 \text{ mA}$$

Determine the maximum value to which V_{CC} can be adjusted without exceeding any rating. Which rating would be exceeded first ?

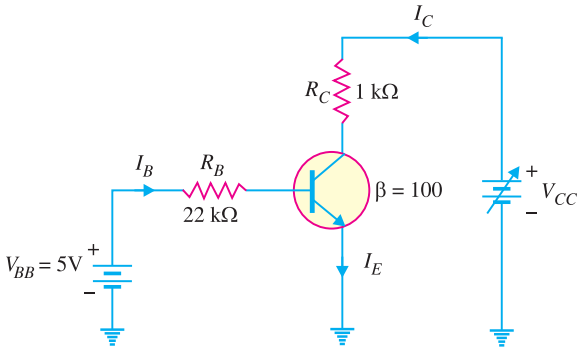


Fig. 8.63

Solution.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{V} - 0.7\text{V}}{22\,k\Omega} = \frac{4.3\,V}{22\,k\Omega} = 195 \text{ μA}$$

$\therefore \quad I_C = \beta I_B = 100 \times 195 \text{ μA} = 19.5$ mA

Note that I_C is much less than $I_{C(max)}$ and will not change with V_{CC}. It is determined only by I_B and β. Therefore, **current rating is not exceeded.**

Now $V_{CC} = V_{CE} + I_C R_C$

We can find the value of V_{CC} when $V_{CE\,(max)} = 15\text{V}$.

$$\therefore \quad V_{CC\,(max)} = V_{CE\,(max)} + I_C R_C$$
$$= 15\text{V} + 19.5 \text{ mA} \times 1 \text{ k}\Omega = 15\text{V} + 19.5 \text{ V} = 34.5\text{V}$$

Therefore, we can increase V_{CC} to **34.5V** before $V_{CE\,(max)}$ is reached.

$$P_D = V_{CE\,(max)} I_C = (15\text{V})\,(19.5 \text{ mA}) = 293 \text{ mW}$$

Since $P_{D\,(max)} = 800$ mW, **it is not exceeded** when $V_{CC} = 34.5\text{V}$.

If base current is removed causing the transistor to turn off, $V_{CE\,(max)}$ **will be exceeded** because the entire supply voltage V_{CC} will be dropped across the transistor.

8.24. Determination of Transistor Configuration

In practical circuits, you must be able to tell whether a given transistor is connected as a common emitter, common base or common collector. There is an easy way to ascertain it. Just locate the terminals where the input a.c. singal is applied to the transistor and where the a.c output is taken from the transistor. The remaining third terminal is the common terminal. For instance, if the a.c input is

applied to the base and the a.c output is taken from the collector, then common terminal is the emitter. Hence the transistor is connected in **common emitter configuration.** If the a.c. input is applied to the base and a.c output is taken from the emitter, then common terminal is the collector. Therefore, the transistor is connected in **common collector configuration.**

8.25 Semiconductor Devices Numbering System

From the time semiconductor engineering came to existence, several numbering systems were adopted by different countries. However, the accepted numbering system is that announced by Proelectron Standardisation Authority in Belgium. According to this system of numbering semiconductor devices :

(i) Every semiconductor device is numbered by five alpha-numeric symbols, comprising either two letters and three numbers (*e.g.* BF194) or three letters and two numbers (*e.g.* BFX63). When two numbers are included in the symbol (*e.g.* BFX63), the device is intended for industrial and professional equipment. When the symbol contains three numbers (*e.g.* BF194) , the device is intended for entertainment or consumer equipment.

(ii) The first letter indicates the nature of semiconductor material. For example :

A = germanium, B = silicon, C = gallium arsenide, R = compound material (e.g. cadmium sulphide)

Thus AC125 is a germanium transistor whereas BC149 is a silicon transistor.

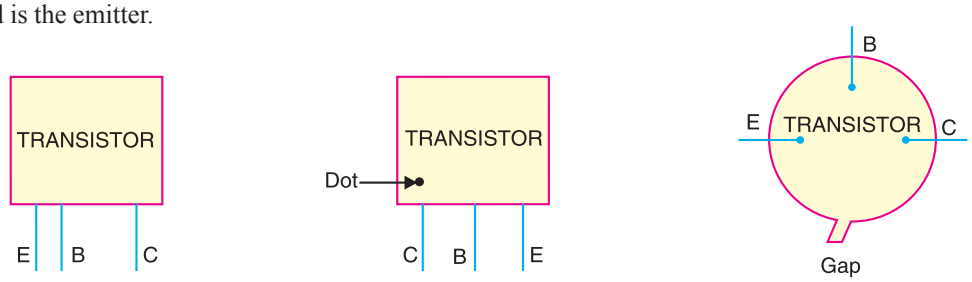
(iii) The second letter indicates the device and circuit function.

A	= diode	*B*	= Variable capacitance diode
C	= A.F. low powered transistor	*D*	= A.F. power transistor
E	= Tunnel diode	*F*	= H.F. low power transistor
G	= Multiple device	*H*	= Magnetic sensitive diode
K	= Hall-effect device	*L*	= H.F. power transistor
M	= Hall-effect modulator	*P*	= Radiation sensitive diode
Q	= Radiation generating diode	*R*	= Thyristor (SCR or triac)
S	= Low power switching transistor	*T*	= Thyristor (power)
U	= Power switching transistor	*X*	= diode, multiplier
Y	= Power device	*Z*	= Zener diode

8.26 Transistor Lead Identification

There are three leads in a transistor *viz*. collector, emitter and base. When a transistor is to be connected in a circuit, it is necessary to know which terminal is which. The identification of the leads of transistor varies with manufacturer. However, there are three systems in general use as shown in Fig. 8.64.

(i) When the leads of a transistor are in the same plane and unevenly spaced [See Fig. 8.64 (*i*)], they are identified by the positions and spacings of leads. The central lead is the base lead. The collector lead is identified by the larger spacing existing between it and the base lead. The remaining lead is the emitter.



(*i*) (*ii*) (*iii*)

Fig. 8.64

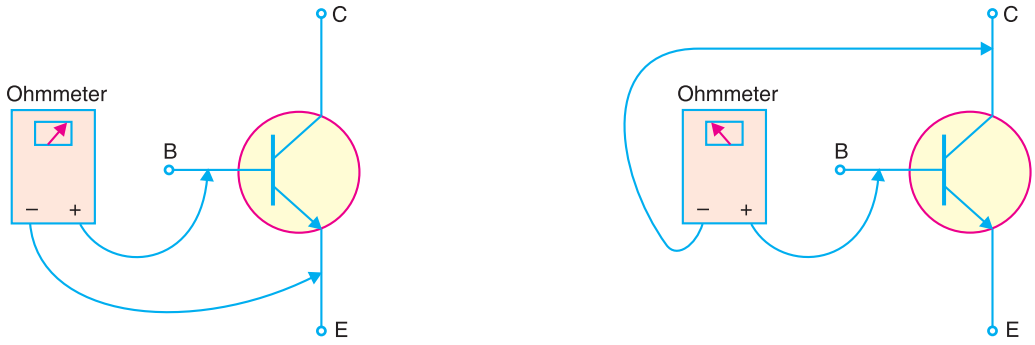
(*ii*) When the leads of a transistor are in the same plane but evenly spaced [See Fig. 8.64 (*ii*)], the central lead is the base, the lead identified by dot is the collector and the remaining lead is the emitter.

(*iii*) When the leads of a transistor are spaced around the circumference of a circle [See Fig. 8.64 (*iii*)], the three leads are generally in E-B-C order clockwise from a gap.

8.27 Transistor Testing

An ohmmeter can be used to check the state of a transistor *i.e.*, whether the transistor is good or not. We know that base-emitter junction of a transistor is forward biased while collector-base junction is reverse biased. Therefore, forward biased base-emitter junction should have low resistance and reverse biased collector-base junction should register a much higher resistance. Fig. 8.65 shows the process of testing an *npn* transistor with an ohmmeter.

(*i*) The forward biased base-emitter junction (biased by internal supply) should read a low resistance, typically 100 Ω to 1 kΩ as shown in Fig. 8.65 (*i*). If that is so, the transistor is good. However, if it fails this check, the transistor is faulty and it must be replaced.



(*i*) (*ii*)

Fig. 8.65

(*ii*) The reverse biased collector-base junction (again reverse biased by internal supply) should be checked as shown in Fig. 8.65 (*ii*). If the reading of the ohmmeter is 100 kΩ or higher, the transistor is good. If the ohmmeter registers a small resistance, the transistor is faulty and requires replacement.

Note. When testing a *pnp* transistor, the ohmmeter leads must be reversed. The results of the tests, however, will be the same.

8.28 Applications of Common Base Amplifiers

Common base amplifiers are not used as frequently as the *CE* amplifiers. The two important applications of *CB* amplifiers are : (*i*) to provide voltage gain without current gain and (*ii*) for impedance matching in high frequency applications. Out of the two, the high frequency applications are far more common.

(*i*) To provide voltage gain without current gain. We know that a *CB* amplifier has a high voltage gain while the current gain is nearly 1 (*i.e.* $A_i \simeq 1$). Therefore, this circuit can be used to provide high voltage gain without increasing the value of circuit current. For instance, consider the case where the output current from an amplifier has sufficient value for the required application but the voltage gain needs to be increased. In that case, *CB* amplifier will serve the purpose because it

would increase the voltage without increasing the current. This is illustrated in Fig. 8.66. The *CB* amplifier will provide voltage gain without any current gain.

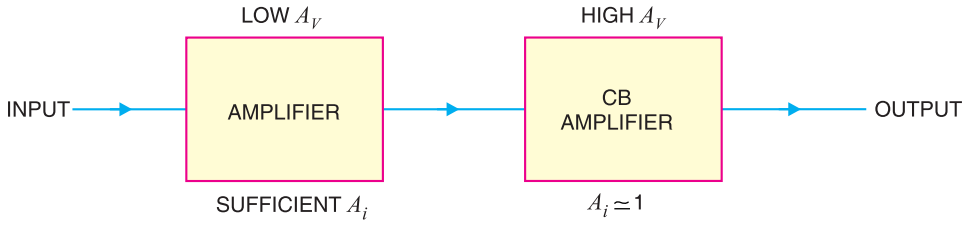


Fig. 8.66

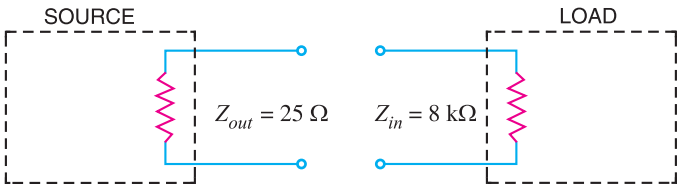


Fig. 8.67

(*ii*) For impedance matching in high frequency applications. Most high-frequency voltage sources have a very *low output impedance*. When such a low-impedance source is to be connected to a high-impedance load, you need a circuit to match the source impedance to the load impedance. Since a common-base amplifier has *low input impedance* and *high output impedance*, the common-base circuit will serve well in this situation. Let us illustrate this point with a numerical example. Suppose a high-frequency source with internal resistance 25 Ω is to be connected to a load of 8 kΩ as shown in Fig. 8.67. If the source is directly connected to the load, small source power will be transferred to the load due to mismatching. However, it is possible to design a *CB* amplifier that has an input impedance of nearly 25 Ω and output impedance of nearly 8 kΩ. If such a *CB* circuit is placed between the source and the load, the source will be matched to the load as shown in Fig. 8.68.

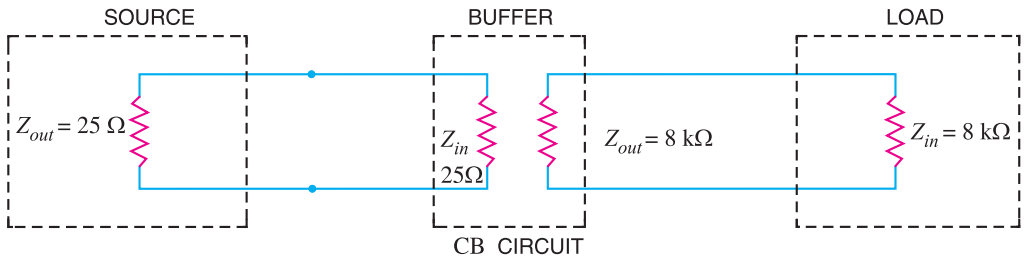


Fig. 8.68

Note that source impedance very closely matches the input impedance of *CB* amplifier. Therefore, there is a maximum power transfer from the source to input of *CB* amplifier. The high output impedance of the amplifier very nearly matches the load resistance. As a result, there is a maximum power transfer from the amplifier to the load. The net result is that maximum power has been transferred from the original source to the original load. A common-base amplifier that is used for this purpose is called a *buffer amplifier*.

8.29 Transistors Versus Vacuum Tubes

Advantages of transistors

A transistor is a solid-state device that performs the same functions as the grid-controlled vacuum tube. However, due to the following advantages, the transistors have upstaged the vacuum tubes in most areas of electronics :

(*i*) High voltage gain. We can get much more voltage gain with a transistor than with a vacuum tube. Triode amplifiers normally have voltage gain of less than 75. On the other hand, transistor amplifiers can provide a voltage gain of 300 or more. This is a distinct advantage of transistors over the tubes.

(*ii*) Lower supply voltage. Vacuum tubes require much higher d.c. voltages than transistors. Vacuum tubes generally run at d.c. voltages ranging from 200V to 400V whereas transistors require much smaller d.c. voltages for their operation. The low voltage requirement permits us to build portable, light-weight transistor equipment instead of heavier vacuum-tube equipment.

(*iii*) No heating. A transistor does not require a heater whereas the vacuum tube can only operate with a heater. The heater requirement in vacuum tubes poses many problems. First, it makes the power supply bulky. Secondly, there is a problem of getting rid of heat. The heater limits the tube's useful life to a few thousand hours. Transistors, on the other hand, last for many years. This is the reason that transistors are permanently soldered into a circuit whereas tubes are plugged into sockets.

(*iv*) Miscellaneous. Apart from the above salient advantages, the transistors have superior edge over the tubes in the following respects :

(*a*) transistors are much smaller than vacuum tubes. This means that transistor circuits can be more compact and light-weight.

(*b*) transistors are mechanically strong due to solid-state.

(*c*) transistors can be integrated along with resistors and diodes to produce *IC*s which are extremely small in size.

Disadvantages of transistors

Although transistors are constantly maintaining superiority over the vacuum tubes, yet they suffer from the following drawbacks :

(*i*) Lower power dissipation. Most power transistors have power dissipation below 300W while vacuum tubes can easily have power dissipation in kW. For this reason, transistors cannot be used in high power applications e.g. transmitters, industrial control systems, microwave systems etc. In such areas, vacuum tubes find wide applications.

(*ii*) Lower input impedance. A transistors has low input impedance. A vacuum tube, on the other hand, has very high input impedance (of the order of MΩ) because the control grid draws negligible current. There are many electronic applications where we required high input impedance *e.g.* electronic voltmeter, oscilloscope etc. Such areas of application need vacuum tubes. It may be noted here that field-effect transistor (*FET*) has a very high input impedance and can replace a vacuum tube in almost all applications.

(*iii*) Temperature dependence. Solid-state devices are very much temperature dependent. A slight change in temperature can cause a significant change in the characteristics of such devices. On the other hand, small variations in temperature hardly affect the performance of tubes. It is a distinct disadvantage of transistors.

(*iv*) Inherent variation of parameters. The manufacture of solid-state devices is indeed a very difficult process. Inspite of best efforts, the parameters of transistors (*e.g.* β, V_{BE} *etc.*) are not the same even for the transistors of the same batch. For example, β for *BC* 148 transistors may vary between 100 and 600.

MULTIPLE-CHOICE QUESTIONS

1. A transistor has .....
(*i*) one *pn* junction
(*ii*) two *pn* junctions
(*iii*) three *pn* junctions
(*iv*) four *pn* junctions

2. The number of depletion layers in a transistor is .....
(*i*) four (*ii*) three
(*iii*) one (*iv*) two

3. The base of a transistor is ..... doped.
(*i*) heavily (*ii*) moderately
(*iii*) lightly (*iv*) none of the above

4. The element that has the biggest size in a transistor is .....
(*i*) collector (*ii*) base
(*iii*) emitter
(*iv*) collector-base junction

5. In a *pnp* transistor, the current carriers are .....
(*i*) acceptor ions (*ii*) donor ions
(*iii*) free electrons (*iv*) holes

6. The collector of a transistor is ..... doped.
(*i*) heavily (*ii*) moderately
(*iii*) lightly (*iv*) none of the above

7. A transistor is a ..... operated device.
(*i*) current (*ii*) voltage
(*iii*) both voltage and current
(*iv*) none of the above

8. In an *npn* transistor, ... are the minority carriers.
(*i*) free electrons (*ii*) holes
(*iii*) donor ions (*iv*) acceptor ions

9. The emitter of a transistor is ..... doped.
(*i*) lightly (*ii*) heavily
(*iii*) moderately (*iv*) none of the above

10. In a transistor, the base current is about ..... of emitter current.
(*i*) 25% (*ii*) 20%
(*iii*) 35% (*iv*) 5%

11. At the base-emitter junction of a transistor, one finds .....
(*i*) reverse bias
(*ii*) a wide depletion layer
(*iii*) low resistance
(*iv*) none of the above

12. The input impedance of a transistor is .....
(*i*) high (*ii*) low
(*iii*) very high (*iv*) almost zero

13. Most of the majority carriers from the emitter .....
(*i*) recombine in the base
(*ii*) recombine in the emitter
(*iii*) pass through the base region to the collector
(*iv*) none of the above

14. The current I_B is .....
(*i*) electron current
(*ii*) hole current
(*iii*) donor ion current
(*iv*) acceptor ion current

15. In a transistor, ...
(*i*) $I_C = I_E + I_B$ (*ii*) $I_B = I_C + I_E$
(*iii*) $I_E = I_C - I_B$ (*iv*) $I_E = I_C + I_B$

16. The value of α of a transistor is .....
(*i*) more than 1 (*ii*) less than 1
(*iii*) 1 (*iv*) none of the above

17. $I_C = \alpha I_E +$ .....
(*i*) I_B (*ii*) I_{CEO}
(*iii*) I_{CBO} (*iv*) βI_B

18. The output impedance of a transistor is .....
(*i*) high (*ii*) zero
(*iii*) low (*iv*) very low

19. In a transistor, I_C = 100 mA and I_E = 100.5 mA. The value of β is .....
(*i*) 100 (*ii*) 50
(*iii*) about 1 (*iv*) 200

20. In a transistor if $\beta = 100$ and collector current is 10 mA, then I_E is .....
(*i*) 100 mA (*ii*) 100.1 mA
(*iii*) 110 mA (*iv*) none of the above

21. The relation between β and α is .....
(*i*) $\beta = \frac{1}{1-\alpha}$ (*ii*) $\beta = \frac{1-\alpha}{\alpha}$
(*iii*) $\beta = \frac{\alpha}{1-\alpha}$ (*iv*) $\beta = \frac{\alpha}{1+\alpha}$

22. The value of β for a transistor is generally .....
(*i*) 1 (*ii*) less than 1
(*iii*) between 20 and 500
(*iv*) above 500

23. The most commonly used transistor arrangement is ..... arrangement.
(*i*) common emitter
(*ii*) common base
(*iii*) common collector
(*iv*) none of the above

24. The input impedance of a transistor connected in ..... arrangement is the highest.
(*i*) common emitter
(*ii*) common collector
(*iii*) common base
(*iv*) none of the above

25. The output impedance of a transistor connected in ..... arrangement is the highest.
(*i*) common emitter
(*ii*) common collector
(*iii*) common base
(*iv*) none of the above

26. The phase difference between the input and output voltages in a common base arrangement is .....
(*i*) 180° (*ii*) 90°
(*iii*) 270° (*iv*) 0°

27. The power gain of a transistor connected in ..... arrangement is the highest.
(*i*) common emitter
(*ii*) common base
(*iii*) common collector
(*iv*) none of the above

28. The phase difference between the input and output voltages of a transistor connected in common emitter arrangement is .....
(*i*) 0° (*ii*) 180°
(*iii*) 90° (*iv*) 270°

29. The voltage gain of a transistor connected in ..... arrangement is the highest.
(*i*) common base (*ii*) common collector
(*iii*) common emitter
(*iv*) none of the above

30. As the temperature of a transistor goes up, the base-emitter resistance .....
(*i*) decreases (*ii*) increases
(*iii*) remains the same
(*iv*) none of the above

31. The voltage gain of a transistor connected in common collector arrangement is .....
(*i*) equal to 1 (*ii*) more than 10
(*iii*) more than 100 (*iv*) less than 1

32. The phase difference between the input and output voltages of a transistor connected in common collector arrangement is .....
(*i*) 180° (*ii*) 0°
(*iii*) 90° (*iv*) 270°

33. $I_C = \beta I_B +$ .....
(*i*) I_{CBO} (*ii*) I_C
(*iii*) I_{CEO} (*iv*) αI_E

34. $I_C = \frac{\alpha}{1-\alpha} I_B +$ .....
(*i*) I_{CEO} (*ii*) I_{CBO}
(*iii*) I_C (*iv*) $(1-\alpha) I_B$

35. $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{.....}{1-\alpha}$
(*i*) I_{CBO} (*ii*) I_{CEO}
(*iii*) I_C (*iv*) I_E

36. BC 147 transistor indicates that it is made of .....
(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) none of the above

37. $I_{CEO} =$ (.....) I_{CBO}
(*i*) β (*ii*) $1 + \alpha$
(*iii*) $1 + \beta$ (*iv*) none of the above

38. A transistor is connected in *CB* mode. If it is now connected in *CE* mode with same bias voltages, the values of I_E, I_B and I_C will ....
(*i*) remain the same
(*ii*) increase
(*iii*) decrease (*iv*) none of the above

39. If the value of α is 0.9, then value of β is .....
(*i*) 9 (*ii*) 0.9
(*iii*) 900 (*iv*) 90

40. In a transistor, signal is transferred from a ..... circuit.
(*i*) high resistance to low resistance
(*ii*) low resistance to high resistance
(*iii*) high resistance to high resistance
(*iv*) low resistance to low resistance

41. The arrow in the symbol of a transistor indicates the direction of .....
(*i*) electron current in the emitter
(*ii*) electron current in the collector
(*iii*) hole current in the emitter
(*iv*) donor ion current

42. The leakage current in *CE* arrangement is

..... that in *CB* arrangement.
(*i*) more than (*ii*) less than
(*iii*) the same as (*iv*) none of the above

43. A heat sink is generally used with a transistor to .....
(*i*) increase the forward current
(*ii*) decrease the forward current
(*iii*) compensate for excessive doping
(*iv*) prevent excessive temperature rise

44. The most commonly used semiconductor in the manufacture of a transistor is .....
(*i*) germanium (*ii*) silicon
(*iii*) carbon (*iv*) none of the above

45. The collector-base junction in a transistor has .....
(*i*) forward bias at all times
(*ii*) reverse bias at all times
(*iii*) low resistance
(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iv*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*iv*)
6. (*ii*)	**7.** (*i*)	**8.** (*ii*)	**9.** (*ii*)	**10.** (*iv*)
11. (*iii*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*i*)	**15.** (*iv*)
16. (*ii*)	**17.** (*iii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*ii*)
21. (*iii*)	**22.** (*iii*)	**23.** (*i*)	**24.** (*ii*)	**25.** (*iii*)
26. (*iv*)	**27.** (*i*)	**28.** (*ii*)	**29.** (*iii*)	**30.** (*i*)
31. (*iv*)	**32.** (*ii*)	**33.** (*iii*)	**34.** (*i*)	**35.** (*i*)
36. (*ii*)	**37.** (*iii*)	**38.** (*i*)	**39.** (*iv*)	**40.** (*ii*)
41. (*iii*)	**42.** (*i*)	**43.** (*iv*)	**44.** (*ii*)	**45.** (*ii*)

Chapter Review Topics

1. What is a transistor ? Why is it so called ?

2. Draw the symbol of *npn* and *pnp* transistor and specify the leads.

3. Show by means of a diagram how you normally connect external batteries in (*i*) *pnp* transistor (*ii*) *npn* transistor.

4. Describe the transistor action in detail.

5. Explain the operation of transistor as an amplifier.

6. Name the three possible transistor connections.

7. Define α. Show that it is always less than unity.

8. Draw the input and output characteristics of *CB* connection. What do you infer from these characteristics ?

9. Define β. Show that : $\beta = \dfrac{\alpha}{1-\alpha}$.

10. How will you determine the input and output characteristics of *CE* connection experimentally ?

11. Establish the following relations :

(*i*) $I_C = \alpha I_E + I_{CBO}$ (*ii*) $I_C = \dfrac{\alpha}{1-\alpha} I_B + \dfrac{1}{1-\alpha} I_{CBO}$

(*iii*) $I_C = \beta I_B + I_{CEO}$ (*iv*) $\gamma = \dfrac{1}{1-\alpha}$

(*v*) $I_E = (\beta + 1) I_B + (\beta + 1) I_{CBO}$

12. How will you draw d.c. load line on the output characteristics of a transistor ? What is its importance?

13. Explain the following terms : (*i*) voltage gain (*ii*) power gain (*iii*) effective collector load.

14. Write short notes on the following : (*i*) advantages of transistors (*ii*) operating point (*iii*) d.c. load line.

Problems

1. In a transistor if $I_C = 4.9$mA and $I_E = 5$mA, what is the value of α ? **[0.98]**
2. In a transistor circuit, $I_E = 1$mA and $I_C = 0.9$mA. What is the value of I_B ? **[0.1 mA]**
3. Find the value of β if $\alpha = 0.99$. **[100]**
4. In a transistor, $\beta = 45$, the voltage across 5kΩ resistance which is connected in the collector circuit is 5 volts. Find the base current. **[0.022 mA]**
5. In a transistor, $I_B = 68\ \mu$A, $I_E = 30$ mA and $\beta = 440$. Find the value of α. Hence determine the value of I_C. **[0.99 ; 29.92 mA]**
6. The maximum collector current that a transistor can carry is 500 mA. If $\beta = 300$, what is the maximum allowable base current for the device ? **[1.67 mA]**
7. For the circuit shown in Fig. 8.69, draw the d.c. load line.

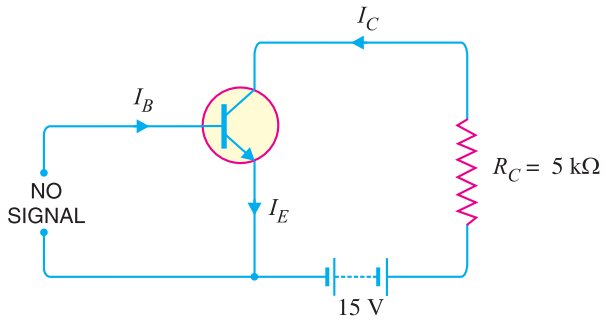


Fig. 8.69

8. Draw the d.c. load line for Fig. 8.70.

[The end points of load line are **6.06 mA** and **20 V]**

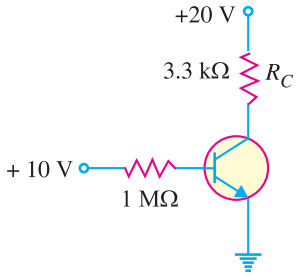


Fig. 8.70

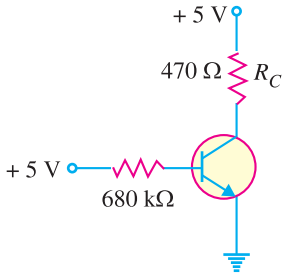


Fig. 8.71

9. If the collector resistance R_C in Fig. 8.70 is reduced to 1 kΩ, what happens to the d.c. load line ?

[The end points of d.c. load line are now **20 mA** and **20 V]**

10. Draw the d.c. load line for Fig. 8.71.

[The end points of d.c. load line are **10.6 mA** and **5V]**

11. If the collector resistance R_C in Fig. 8.71 is increased to 1 kΩ, what happens to the d.c. load line ?

[The end points of d.c. load line are now **5 mA** and **5 V]**

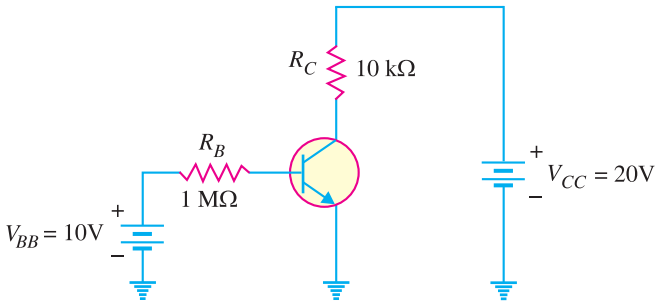


Fig. 8.72

12. Determine the intercept points of the d.c. load line on the vertical and horizontal axes of the collector curves in Fig. 8.72. **[2 mA ; 20 V]**

13. For the circuit shown in Fig. 8.73, find (*i*) the state of the transistor and (*ii*) transistor power. **[(*i*) active (*ii*) 4.52 mW]**

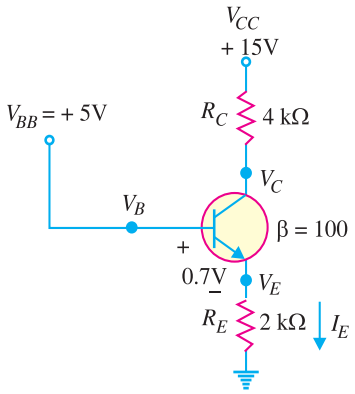


Fig. 8.73

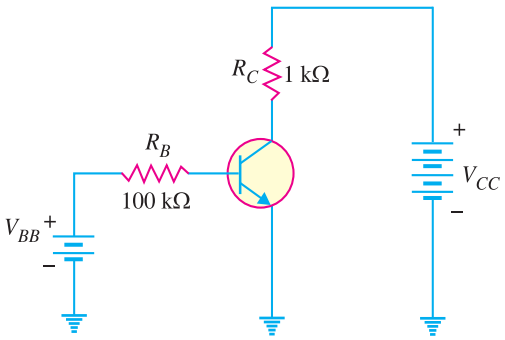


Fig. 8.74

14. A base current of 50 μA is applied to the transistor in Fig. 8.74 and a voltage of 5V is dropped across R_C. Calculate α for the transistor. **[0.99]**

15. A certain transistor is to be operated at a collector current of 50 mA. How high can V_{CE} go without exceeding $P_{D\,(max)}$ of 1.2 W ? **[24 V]**

Discussion Questions

1. Why is a transistor low powered device ?
2. What is the significance of arrow in the transistor symbol ?
3. Why is collector wider than emitter and base ?
4. Why is collector current slightly less than emitter current ?
5. Why is base made thin ?

Top

Contents

19

Field Effect Transistors

INTRODUCTION

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The *FET* is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding *FET* market has led many semiconductor market-

ing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET.*

19.2 Junction Field Effect Transistor (JFET)

A **junction field effect transistor** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (*ii*). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).

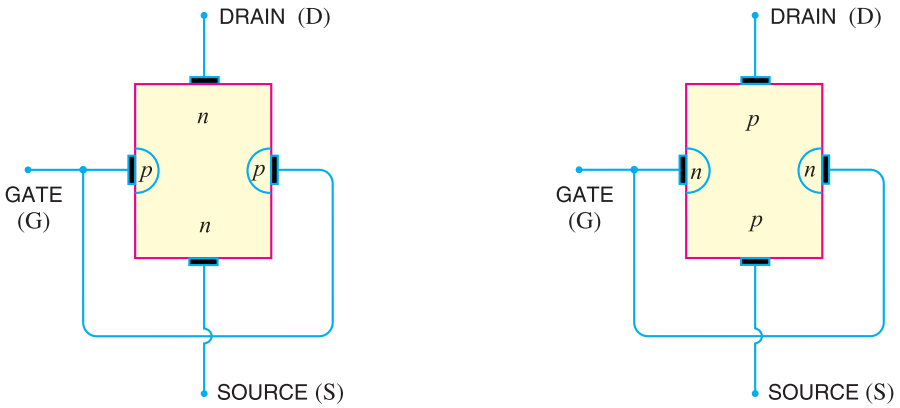


Fig. 19.1

* It would seem from Fig. 19.1 that there are three doped material regions. However, this is not the case. The gate material *surrounds* the channel in the same manner as a belt surrounding your waist.

JFET polarities. Fig. 19.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 19.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

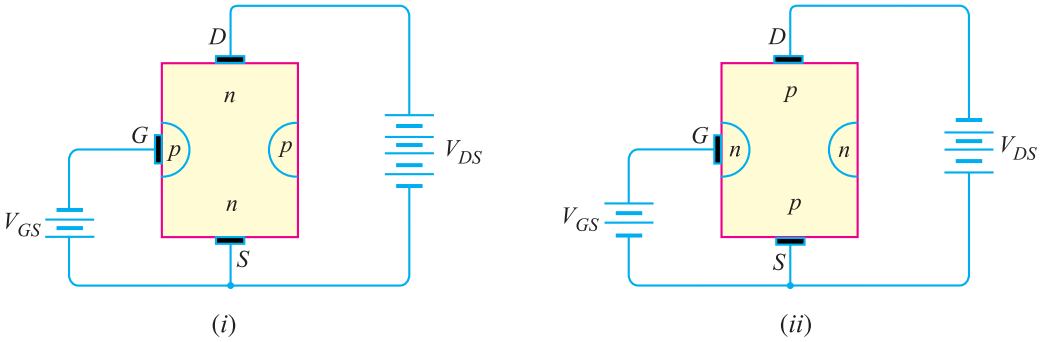


Fig. 19.2

The following points may be noted :

(*i*) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

(*ii*) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

(*iii*) In all *JFETs*, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

Fig. 19.3 shows the circuit of *n*-channel *JFET* with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence *resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.* In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Working. The working of *JFET* is as under :

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

* The resistance of the channel depends upon its area of X-section. The greater the X-sectional area of this channel, the lower will be its resistance and the greater will be the current flow through it.

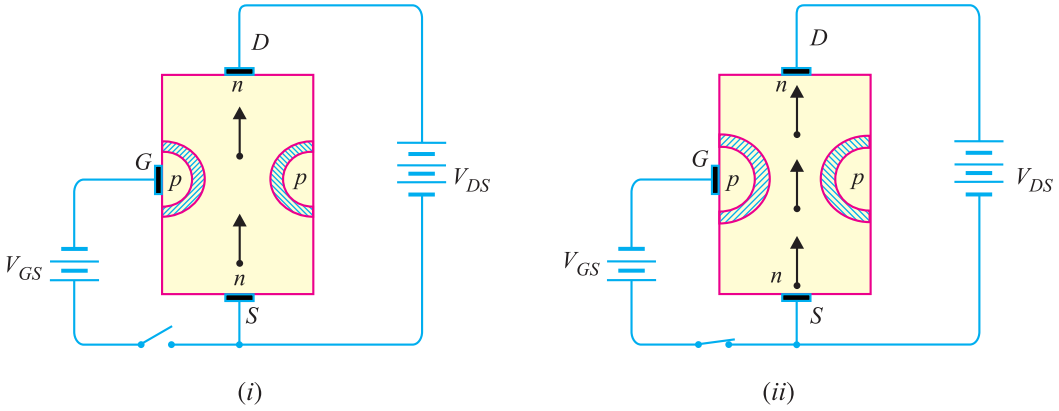
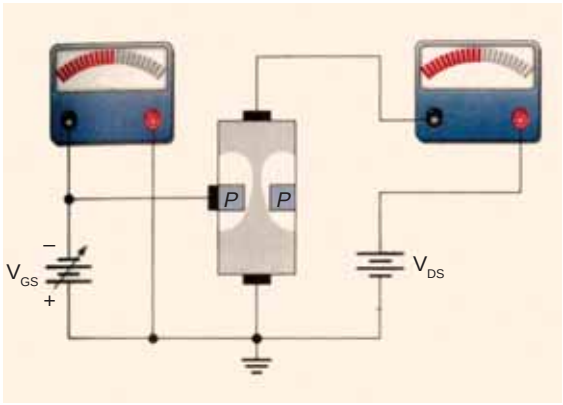


Fig. 19.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

Note. If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel becomes a non-conductor.



JFET biased for Conduction

19.4 Schematic Symbol of JFET

Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought

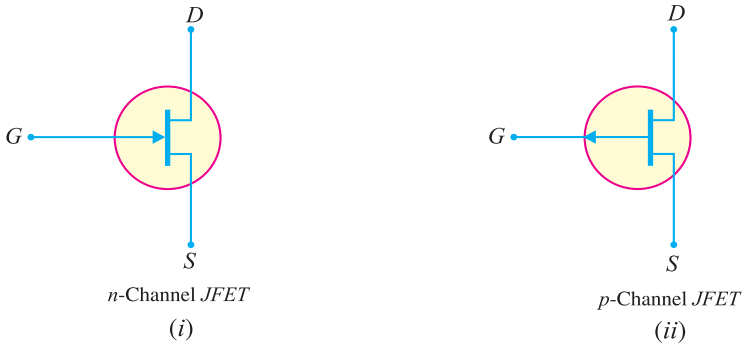
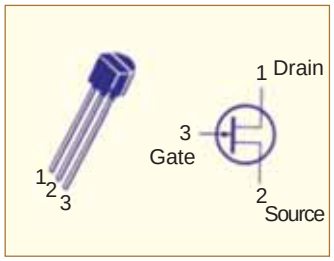


Fig. 19.4

as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (*ii*)].



19.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0$A). However, typical *BJT* base current might be a few μA while *JFET* gate current a thousand times smaller [See Fig. 19.5].

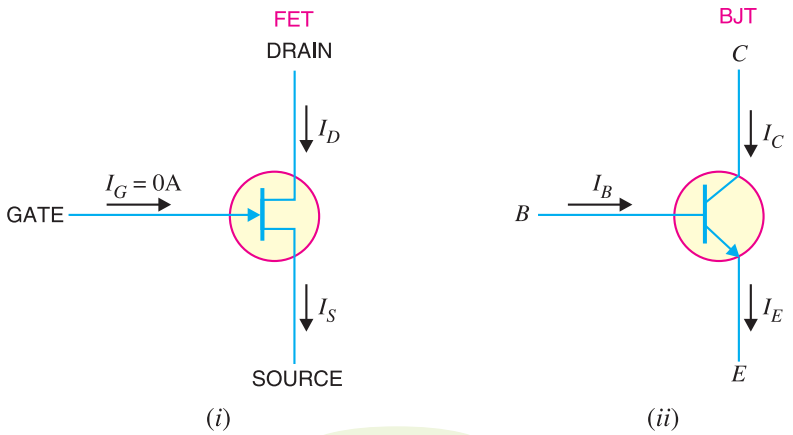


Fig. 19.5

* The gate, source and drain of a *JFET* correspond to grid, cathode and anode of a vacuum tube.

(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

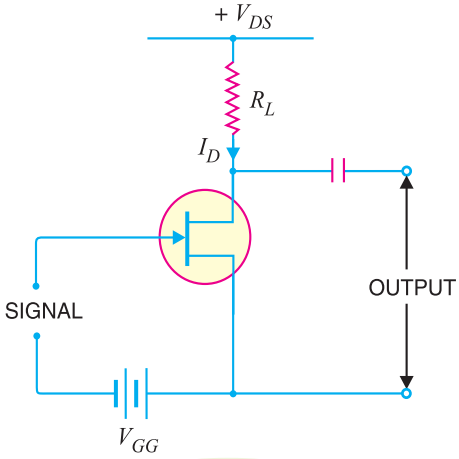


Fig. 19.6

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

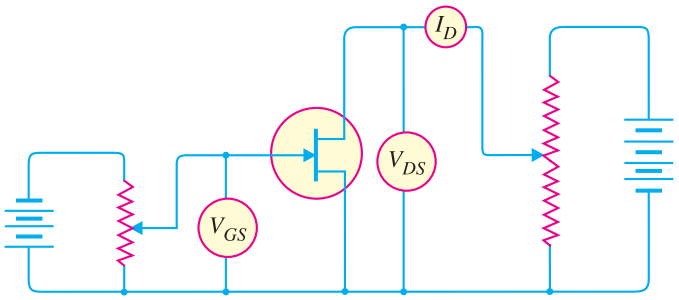


Fig. 19.7

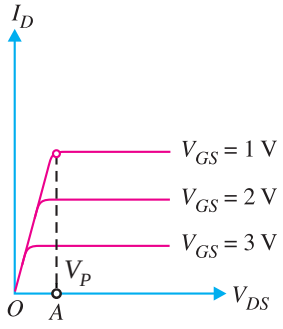


Fig. 19.8

The following points may be noted from the characteristics :

(*i*) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 19.8, *OA* is the *pinch off voltage* V_P.

(*ii*) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(*iii*) The characteristics resemble that of a pentode valve.

19.9 Salient Features of JFET

The following are some salient features of *JFET* :

(*i*) A *JFET* is a three-terminal *voltage-controlled* semiconductor device *i.e.* input voltage controls the output characteristics of *JFET.*

(*ii*) The *JFET* is *always* operated with gate-source *pn* junction *reverse biased.

(*iii*) In a *JFET*, the gate current is zero *i.e.* $I_G = 0$A.

(*iv*) Since there is no gate current, $I_D = I_S$.

(*v*) The *JFET* must be operated between V_{GS} and $V_{GS\,(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

(*vi*) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(*vii*) The *JFET* is not subjected to thermal runaway when the temperature of the device increases.

(*viii*) The drain current I_D is controlled by changing the channel width.

(*ix*) Since *JFET* has no gate current, there is no β rating of the device. We can find drain current I_D by using the eq. mentioned in Art. 19.11.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS\,(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current*.

Fig 19.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

* Forward biasing gate-source *pn* junction may destroy the device.

** When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

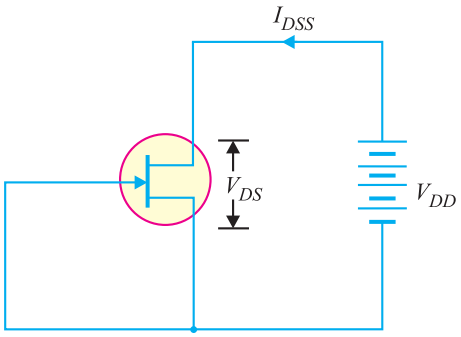


Fig. 19.9

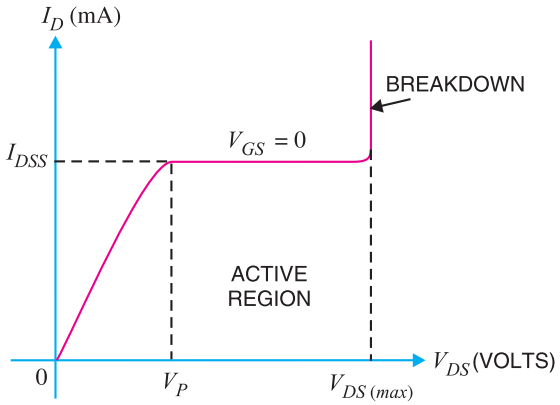


Fig. 19.10

The following points may be noted carefully :

(*i*) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(*ii*) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 19.10.

(*iii*) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or *active region*. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 19.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for $V_{GS} = 0$V, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

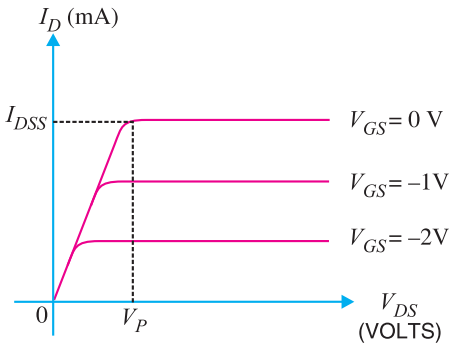


Fig . 19.11

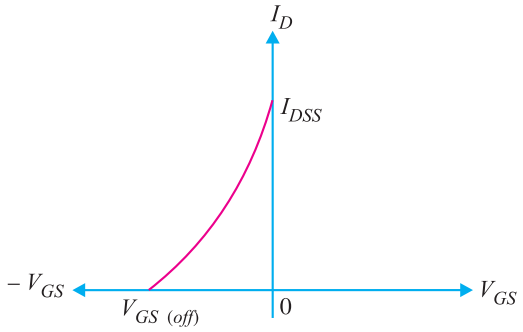


Fig . 19.12

3. Gate-source cut off voltage $V_{GS\ (off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 19.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\,(off)}$.

Notes. (*i*) It is interesting to note that $V_{GS\ (off)}$ will always have the same magnitude value as V_P. For example if $V_P = 6$ V, then $V_{GS\ (off)} = -6$ V. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_P and $V_{GS\,(off)}$. Note that V_P is the value of V_{DS} that causes the *JEFT* to become a constant current device. It is measured at $V_{GS} = 0$ V and will have a constant drain current = I_{DSS}. However, $V_{GS\ (off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

19.11 Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 19.13. We note that gate-source cut off voltage [*i.e.* $V_{GS\,(off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = |V_{GS\,(off)}|$$

For example, if a *JFET* has $V_{GS\,(off)} = -4$V, then $V_P = 4$V.

The transfer characteristic of *JFET* shown in Fig. 19.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where
I_D = drain current at given V_{GS}
I_{DSS} = shorted – gate drain current
V_{GS} = gate–source voltage
$V_{GS\,(off)}$ = gate–source cut off voltage

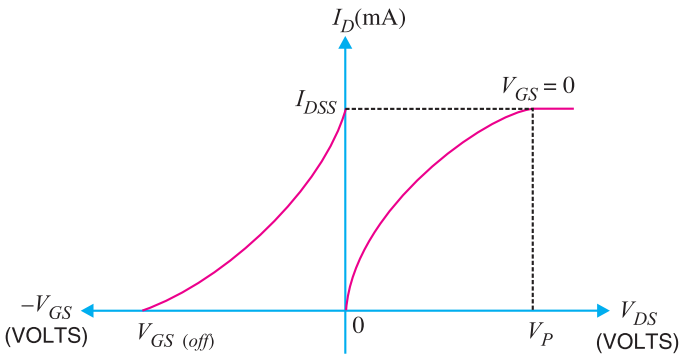


Fig. 19.13

Example 19.1. *Fig. 19.14 shows the transfer characteristic curve of a JFET. Write the equation for drain current.*

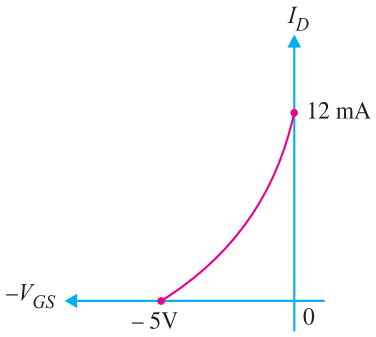


Fig. 19.14

Solution. Referring to the transfer characteristic curve in Fig. 19.14, we have,

$$I_{DSS} = 12 \text{ mA}$$

$$V_{GS\,(off)} = -5 \text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or $$I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA}$$ **Ans.**

Example 19.2. *A JFET has the following parameters: $I_{DSS} = 32$ mA ; $V_{GS\,(off)} = -8$V ; $V_{GS} = -4.5$ V. Find the value of drain current.*

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$

$$= \mathbf{6.12 \text{ mA}}$$

Example 19.3. *A JFET has a drain current of 5 mA. If $I_{DSS} = 10$ mA and $V_{GS\,(off)} = -6$ V, find the value of (i) V_{GS} and (ii) V_P.*

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or $$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

or $$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(*i*) $\therefore \quad V_{GS} = \mathbf{-1.76 \text{ V}}$

(*ii*) and $$V_P = -V_{GS\,(off)} = \mathbf{6 \text{ V}}$$

Example 19.4. *For the JFET in Fig. 19.15, $V_{GS\,(off)} = -4$V and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

Solution. Since $V_{GS\,(off)} = -4$V, $V_P = 4$V. The minimum value of V_{DS} for the *JFET* to be in constant-current region is

$$V_{DS} = V_P = 4\text{V}$$

In the constant current region with $V_{GS} = 0$V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$

$$= 4\text{V} + (12 \text{ mA})\,(560\Omega) = 4\text{V} + 6.72\text{V} = \mathbf{10.72\text{V}}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

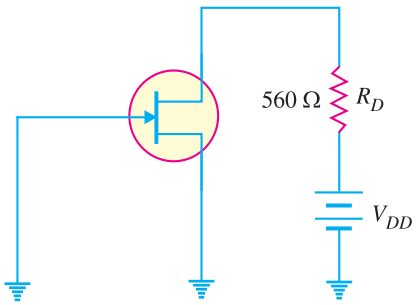


Fig. 19.15

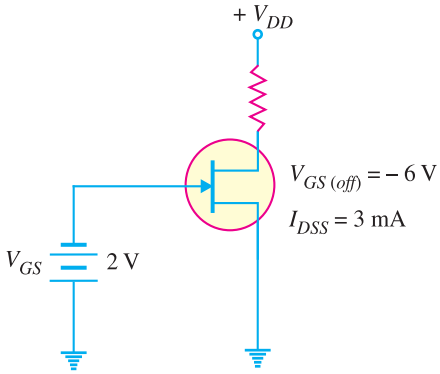


Fig. 19.16

Example 19.5. *Determine the value of drain current for the circuit shown in Fig. 19.16.*

Solution. It is clear from Fig. 19.16 that $V_{GS} = -2$V. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\text{ mA}\left(1 - \frac{-2\text{V}}{-6\text{V}}\right)^2$$

$$= (3\text{ mA})\,(0.444) = \mathbf{1.33\text{ mA}}$$

Example 19.6. *A particular p-channel JFET has a* $V_{GS\,(off)} = +4$*V. What is* I_D *when* $V_{GS} = +6$*V?*

Solution. The *p*-channel *JFET* requires a positive gate-to-source voltage to pass drain current I_D. The more the positive voltage, the less the drain current. When $V_{GS} = 4$V, $I_D = 0$ and *JFET* is cut off. Any further increase in V_{GS} keeps the *JFET* cut off. Therefore, at $V_{GS} = +6$V, $I_D = \mathbf{0A.}$

19.12 Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(*i*) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(*ii*) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(*iii*) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(*iv*) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(*v*) A *JFET* has a smaller size, longer life and high efficiency.

19.13 Parameters of JFET

Like vacuum tubes, a *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are *(i)* a.c. drain resistance *(ii)* transconductance *(iii)* amplification factor.

(*i*) a.c. drain resistance (r_d). Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :

It is the ratio of change in drain-source voltage (ΔV_{DS}) *to the change in drain current* (ΔI_D) *at constant gate-source voltage i.e.*

$$\text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then,

$$\text{a.c. drain resistance, } r_d = \frac{2 \text{ V}}{0.02 \text{ mA}} = 100 \text{ k}\Omega$$

Referring to the output characteristics of a *JFET* in Fig. 19.8, it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat. Therefore, drain resistance of a *JFET* has a large value, ranging from 10 kΩ to 1 MΩ.

(*ii*) Transconductance (g_{fs}). The control that the gate voltage has over the drain current is measured by transconductance g_{fs} and is similar to the transconductance g_m of the tube. It may be defined as follows :

It is the ratio of change in drain current (ΔI_D) *to the change in gate-source voltage* (ΔV_{GS}) *at constant drain-source voltage i.e.*

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then,

$$\text{Transconductance, } g_{fs} = \frac{0.3 \text{ mA}}{0.1 \text{ V}} = 3 \text{ mA/V} = 3 \times 10^{-3} \text{ A/V or mho or } S \text{ (siemens)}$$

$$= 3 \times 10^{-3} \times 10^{6} \text{ μ mho} = 3000 \text{ μ mho (or μS)}$$

(*iii*) Amplification factor (μ). *It is the ratio of change in drain-source voltage* (ΔV_{DS}) *to the change in gate-source voltage* (ΔV_{GS}) *at constant drain current i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a *JFET* is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

19.14 Relation Among JFET Parameters

The relationship among *JFET* parameters can be established as under :

$$\text{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance × transconductance

Example 19.7. *When a reverse gate voltage of 15 V is applied to a JFET, the gate current is* 10^{-3} *μA. Find the resistance between gate and source.*

Solution. $V_{GS} = 15 \text{ V}$; $I_G = 10^{-3} \text{ μA} = 10^{-9} \text{ A}$

$$\therefore \quad \text{Gate to source resistance} = \frac{V_{GS}}{I_G} = \frac{15\text{ V}}{10^{-9}\text{ A}} = 15 \times 10^9\ \Omega = \textbf{15,000 M}\Omega$$

This example shows the major difference between a *JFET* and a bipolar transistor. Whereas the input impedance of a *JFET* is several hundred MΩ, the input impedance of a bipolar transistor is only hundreds or thousands of ohms. The large input impedance of a *JFET* permits high degree of isolation between the input and output.

Example 19.8. *When V_{GS} of a JFET changes from –3.1 V to –3 V, the drain current changes from 1 mA to 1.3 mA. What is the value of transconductance ?*

Solution.

$$\Delta V_{GS} = 3.1 - 3 = 0.1\text{ V} \quad \text{... magnitude}$$

$$\Delta I_D = 1.3 - 1 = 0.3\text{ mA}$$

$$\therefore \quad \text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3\text{ mA}}{0.1\text{ V}} = 3\text{ mA/V} = \textbf{3000 μ mho}$$

Example 19.9. *The following readings were obtained experimentally from a JFET :*

V_{GS}	*0 V*	*0 V*	*– 0.2 V*
V_{DS}	*7 V*	*15 V*	*15 V*
I_D	*10 mA*	*10.25 mA*	*9.65 mA*

Determine (i) a. c. drain resistance (ii) transconductance and (iii) amplification factor.

Solution. (*i*) With V_{GS} constant at 0V, the increase in V_{DS} from 7 V to 15 V increases the drain current from 10 mA to 10.25 mA *i.e.*

$$\text{Change in drain-source voltage, } \Delta V_{DS} = 15 - 7 = 8\text{ V}$$

$$\text{Change in drain current, } \Delta I_D = 10.25 - 10 = 0.25\text{ mA}$$

$$\therefore \quad \text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{8\text{ V}}{0.25\text{ mA}} = \textbf{32 k}\Omega$$

(*ii*) With V_{DS} constant at 15 V, drain current changes from 10.25 mA to 9.65 mA as V_{GS} is changed from 0 V to – 0.2 V.

$$\Delta V_{GS} = 0.2 - 0 = 0.2\text{ V}$$

$$\Delta I_D = 10.25 - 9.65 = 0.6\text{ mA}$$

$$\therefore \quad \text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.6\text{ mA}}{0.2\text{ V}} = 3\text{ mA/V} = \textbf{3000 μ mho}$$

(*iii*) $$\text{Amplification factor, } \mu = r_d \times g_{fs} = (32 \times 10^3) \times (3000 \times 10^{-6}) = \textbf{96}$$

19.15 Variation of Transconductance (g_m or g_{fs}) of JFET

We have seen that transconductance g_m of a *JFET* is the ratio of a change in drain current (ΔI_D) to a change in gate-source voltage (ΔV_{GS}) at constant V_{DS} *i.e.*

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The transconductance g_m of a *JFET* is an important parameter because it is a major factor in determining the voltage gain of *JFET* amplifiers. However, the transfer characteristic curve for a *JFET* is nonlinear so that the value of g_m depends upon the location on the curve. Thus the value of g_m at point *A* in Fig. 19.17 will be different from that at point *B*. Luckily, there is following equation to determine the value of g_m at a specified value of V_{GS} :

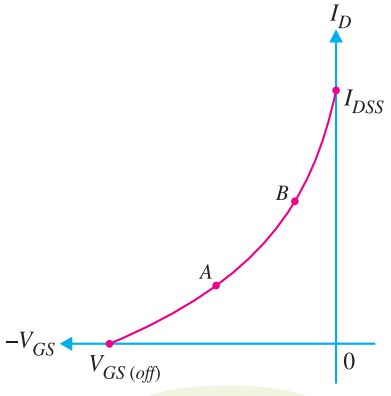


Fig. 19.17

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)$$

where g_m = value of transconductance at any point on the transfer characteristic curve

g_{mo} = value of transconductance(maximum) at $V_{GS} = 0$

Normally, the data sheet provides the value of g_{mo}. When the value of g_{mo} is not available, you can approximately calculate g_{mo} using the following relation :

$$g_{mo} = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|}$$

Example 19.10. *A JFET has a value of g_{mo} = 4000 μS. Determine the value of g_m at V_{GS} = – 3V. Given that $V_{GS\,(off)}$ = – 8V.*

Solution.

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= 4000\ \mu S\left(1 - \frac{-3V}{-8V}\right)$$

$$= 4000\ \mu S\ (0.625) = \mathbf{2500\ \mu S}$$

Example 19.11. *The data sheet of a JFET gives the following information : I_{DSS} = 3 mA, $V_{GS\,(off)}$ = – 6V and $g_{m\,(max)}$ = 5000 μS. Determine the transconductance for V_{GS} = – 4V and find drain current I_D at this point.*

Solution. At $V_{GS} = 0$, the value of g_m is maximum *i.e.* g_{mo}.

$\therefore$ $g_{mo} = 5000\ \mu S$

Now $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)$

$= 5000\ \mu S\left(1 - \frac{-4V}{-6V}\right)$

$= 5000\ \mu S\ (1/3) = \mathbf{1667\ \mu S}$

Also $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$

$= 3\ mA\left(1 - \frac{-4}{-6}\right)^2 = \mathbf{333\ \mu A}$

19.16 JFET Biasing

For the proper operation of *n*-channel *JFET*, gate must be negative *w.r.t.* source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias battery. In this method, *JFET* is biased by a bias battery V_{GG}. This battery ensures that gate is always negative *w.r.t.* source during all parts of the signal.

2. Biasing circuit. The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are (*i*) self-bias (*ii*) potential divider method. We shall discuss each method in turn.

19.17 JFET Biasing by Bias Battery

Fig. 19.18 shows the biasing of a *n*-channel *JFET* by a bias battery $-V_{GG}$. This method is also called *gate bias*. The battery voltage $-V_{GG}$ ensures that gate – source junction remains reverse biased.

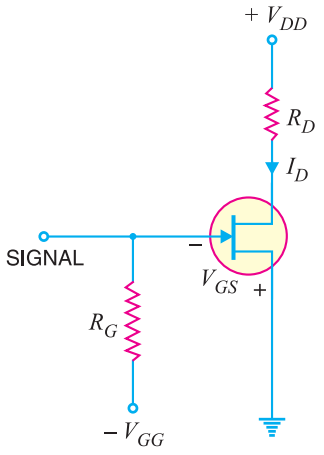


Fig. 19.18

Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \quad V_{GS} = V_{GG}$$

We can find the value of drain current I_D from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

The value of V_{DS} is given by ;

$$V_{DS} = V_{DD} - I_D R_D$$

Thus the d.c. values of I_D and V_{DS} stand determined. The operating point for the circuit is V_{DS}, I_D.

Example 19.12. *A JFET in Fig. 19.19 has values of $V_{GS\,(off)} = -8$V and $I_{DSS} = 16$ mA. Determine the values of V_{GS}, I_D and V_{DS} for the circuit.*

Solution. Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \quad V_{GS} = V_{GG} = \mathbf{-5V}$$

Now

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 16\text{ mA}\left(1 - \frac{-5}{-8}\right)^2$$

$$= 16\text{ mA}\,(0.1406) = \mathbf{2.25\ mA}$$

Also

$$V_{DS} = V_{DD} - I_D R_D$$

$$= 10\text{ V} - 2.25\text{ mA} \times 2.2\text{ k}\Omega = \mathbf{5.05\ V}$$

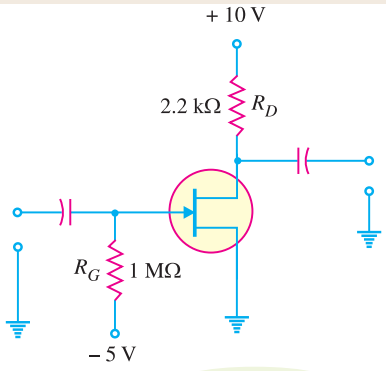


Fig. 19.19

Note that operating point for the circuit is 5.05V, 2.25 mA.

19.18 Self-Bias for JFET

Fig. 19.20 shows the self-bias method for *n*-channel *JFET*. The resistor R_S is the bias resistor. The d.c. component of drain current flowing through R_S produces the desired bias voltage.

$$\text{Voltage across } R_S,\ V_S = I_D R_S$$

Since gate current is negligibly small, the gate terminal is at d.c. ground *i.e.*, $V_G = 0$.

$$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S$$

or

$$V_{GS} = -{}^{*}I_D R_S$$

Thus bias voltage V_{GS} keeps gate negative *w.r.t.* source.

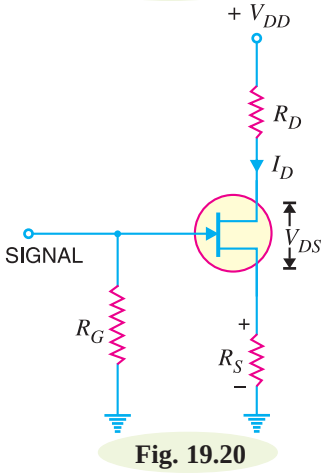


Fig. 19.20

* $V_{GS} = V_G - V_S$ = Negative. This means that V_G is negative w.r.t. V_S. Thus if $V_G = 2$V and $V_S = 4$V, then $V_{GS} = 2 - 4 = -2$V *i.e.* gate is less positive than the source. Again if $V_G = 0$V and $V_S = 2$V, then $V_{GS} = 0 - 2 = -2$V. Note that V_G is less positive than V_S.

Operating point. The operating point (*i.e.*, zero signal I_D and V_{DS}) can be easily determined. Since the parameters of the *JFET* are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Also $$V_{DS} = V_{DD} - I_D\,(R_D + R_S)$$

Thus d.c. conditions of *JFET* amplifier are fully specified *i.e.* operating point for the circuit is V_{DS}, I_D.

Also, $$R_S = \frac{|V_{GS}|}{|I_D|}$$

Note that gate resistor *R_G does not affect bias because voltage across it is zero.

Midpoint Bias. It is often desirable to bias a *JFET* near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. When signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0. It can be proved that when $V_{GS} = V_{GS\,(off)}/3.4$, midpoint bias conditions are obtained for I_D.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS\,(off)}/3.4}{V_{GS\,(off)}}\right)^2 = 0.5\,I_{DSS}$$

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.

Example 19.13. *Find V_{DS} and V_{GS} in Fig. 19.21, given that I_D = 5 mA.*

Solution.

$$V_S = I_D R_S = (5\text{ mA})\,(470\ \Omega) = 2.35\text{ V}$$

and $$V_D = V_{DD} - I_D R_D$$

$$= 15\text{V} - (5\text{ mA}) \times (1\text{ k}\Omega) = 10\text{V}$$

$$\therefore \quad V_{DS} = V_D - V_S = 10\text{V} - 2.35\text{ V} = \mathbf{7.65V}$$

Since there is no gate current, there will be no voltage drop across R_G and $V_G = 0$.

Now $$V_{GS} = V_G - V_S = 0 - 2.35\text{V} = \mathbf{-\,2.35\ V}$$

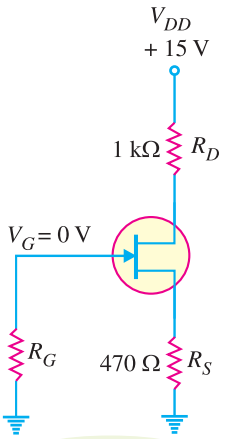


Fig. 19.21

Example 19.14. *The transfer characteristic of a JFET reveals that when V_{GS} = – 5V, I_D = 6.25 mA. Determine the value of R_S required.*

Solution.

$$R_S = \frac{|V_{GS}|}{|I_D|} = \frac{5\text{V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$$

Example 19.15. *Determine the value of R_S required to self-bias a p-channel JFET with I_{DSS} = 25 mA, $V_{GS\,(off)}$ = 15 V and V_{GS} = 5V.*

Solution.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 = 25\text{ mA}\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2 = 25\text{mA}\ (1 - 0.333)^2 = 11.1\text{ mA}$$

$$\therefore \quad R_S = \frac{|V_{GS}|}{|I_D|} = \frac{5\text{V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$$

* R_G is necessary only to isolate an a.c. signal from ground in amplifier applications.

Example 19.16. *Select resistor values in Fig. 19.22 to set up an approximate midpoint bias. The JFET parameters are : I_{DSS} = 15 mA and $V_{GS\,(off)}$ = – 8V. The voltage V_D should be 6V (one-half of V_{DD}).*

Solution. For midpoint bias, we have,

$$I_D \simeq \frac{I_{DSS}}{2} = \frac{15\text{ mA}}{2} = 7.5\text{ mA}$$

and $$V_{GS} = \frac{V_{GS\,(off)}}{3.4} = \frac{-8}{3.4} = -2.35\text{ V}$$

$$\therefore \quad R_S = \frac{|V_{GS}|}{|I_D|} = \frac{2.35\text{V}}{7.5\text{ mA}} = \mathbf{313\Omega}$$

Now $$V_D = V_{DD} - I_D R_D$$

$$\therefore \quad R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12\text{V} - 6\text{V}}{7.5\text{ mA}} = \mathbf{800\Omega}$$

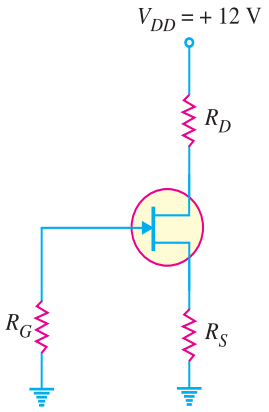


Fig. 19.22

Example 19.17. *In a self-bias n-channel JFET, the operating point is to be set at I_D = 1.5 mA and V_{DS} =10 V. The JFET parameters are I_{DSS} = 5 mA and $V_{GS\,(off)}$ = – 2 V. Find the values of R_S and R_D. Given that V_{DD} = 20 V.*

Solution. Fig. 19.23 shows the circuit arrangement.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

or $$1.5 = 5\left(1 + \frac{V_{GS}}{2}\right)^2$$

or $$1 + \frac{V_{GS}}{2} = \sqrt{1.5/5} = 0.55$$

or $$V_{GS} = -0.9\text{ V}$$

Now $$V_{GS} = V_G - V_S$$

or $$V_S = V_G - V_{GS}$$
$$= 0 - (-0.9) = 0.9\text{ V}$$

$$\therefore \quad R_S = \frac{V_S}{I_D} = \frac{0.9\text{ V}}{1.5\text{ mA}} = \mathbf{0.6\text{ k}\Omega}$$

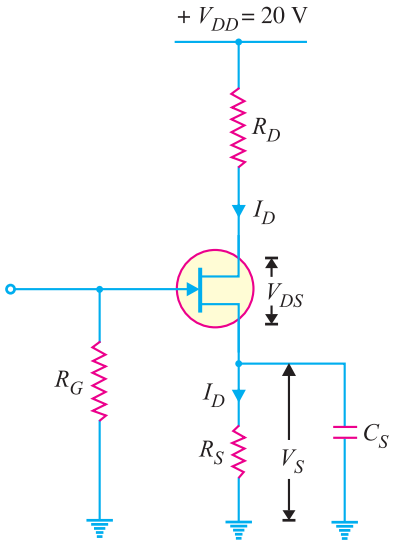


Fig. 19.23

Applying Kirchhoff's voltage law to the drain circuit, we have,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or $$20 = 1.5\text{ mA} \times R_D + 10 + 0.9$$

$$\therefore \quad R_D = \frac{(20 - 10 - 0.9)\text{ V}}{1.5\text{ mA}} = \mathbf{6\text{ k}\Omega}$$

Example 19.18. *In the JFET circuit shown in Fig. 19.24, find (i) V_{DS} and (ii) V_{GS} .*

Solution.

(i) $$V_{DS} = V_{DD} - I_D (R_D + R_S) = 30 - 2.5\text{ mA}\,(5 + 0.2) = 30 - 13 = \mathbf{17\text{ V}}$$

(ii) $$V_{GS} = -I_D R_S = -(2.5 \times 10^{-3}) \times 200 = \mathbf{-0.5\text{ V}}$$

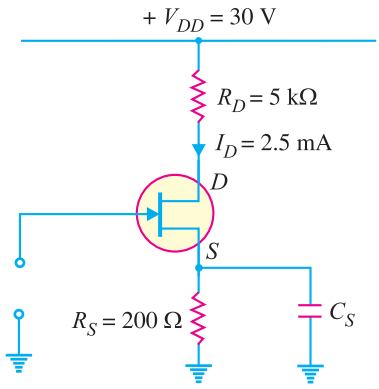


Fig. 19.24

Example 19.19. *Figure 19.25 shows two stages of JFET amplifier. The first stage has I_D = 2.15mA and the second stage has I_D = 9.15mA. Find the d.c. voltage of drain and source of each stage w.r.t. ground.*

Solution. Voltage drop in 8.2 kΩ = 2.15 mA × 8.2 kΩ = 17.63 V

D.C. potential of drain of first stage *w.r.t.* ground is

$$V_D = V_{DD} - 17.63 = 30 - 17.63 = \mathbf{12.37\ V}$$

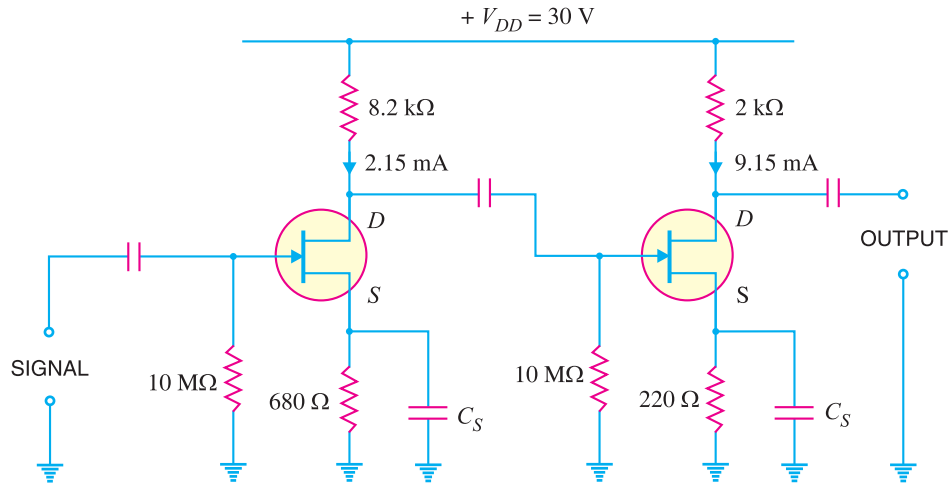


Fig. 19.25

D.C. potential of source of first stage to ground is

$$V_S = I_D R_S = 2.15\ \text{mA} \times 0.68\ \text{k}\Omega = \mathbf{1.46\ V}$$

Voltage drop in 2 kΩ = 9.15 mA × 2 kΩ = 18.3 V

D.C. potential of drain of second stage to ground is

$$V_D = V_{DD} - 18.3 = 30 - 18.3 = \mathbf{11.7\ V}$$

D.C. potential of source of second stage to ground is

$$V_S = I_D R_S = 9.15 \text{ mA} \times 0.22 \text{ k}\Omega = \mathbf{2.01 \text{ V}}$$

19.19 JFET with Voltage-Divider Bias

Fig. 19.26 shows potential divider method of biasing a *JFET*. This circuit is identical to that used for a transistor. The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 (= V_G)across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$V_{GS} = V_2 - I_D R_S$$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under :

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point. The input impedance Z_i of this circuit is given by ;

$$Z_i = R_1 \| R_2$$

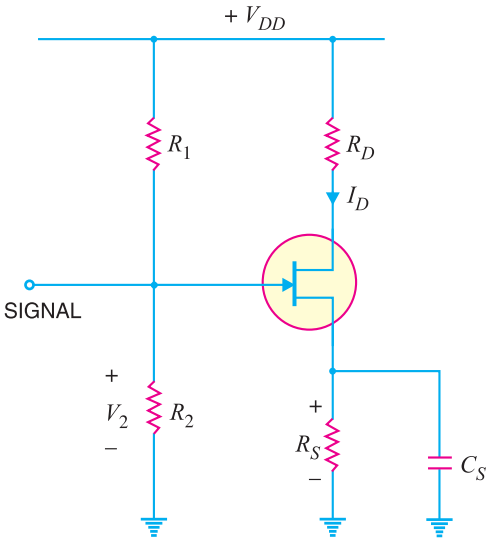


Fig. 19.26

Example 19.20. *Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig. 19.27, given that V_D = 7V.*

Solution.

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{V} - 7\text{V}}{3.3 \text{ k}\Omega}$$

$$= \frac{5\text{V}}{3.3 \text{ k}\Omega} = \mathbf{1.52 \text{ mA}}$$

$$V_S = I_D R_S = (1.52 \text{ mA})\ (1.8 \text{ k}\Omega) = 2.74\text{V}$$

$$V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{12\text{V}}{7.8 \text{ M}\Omega} \times 1 \text{ M}\Omega = 1.54\text{V}$$

$$\therefore \quad V_{GS} = V_G - V_S = 1.54 \text{ V} - 2.74 \text{ V} = \mathbf{-1.2\text{V}}$$

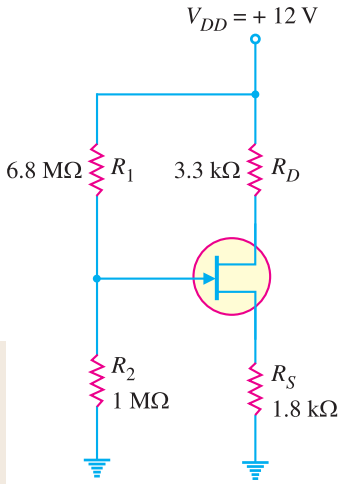


Fig. 19.27

Example 19.21. *In an n-channel JFET biased by potential divider method, it is desired to set the operating point at I_D = 2.5 mA and V_{DS} = 8V. If V_{DD} = 30 V, R_1 = 1 MΩ and R_2 = 500 kΩ, find the value of R_S. The parameters of JFET are I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 5 V.*

Solution. Fig. 19.28 shows the conditions of the problem.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

or $$2.5 = 10\left(1 + \frac{V_{GS}}{5}\right)^2$$

or $$1 + \frac{V_{GS}}{5} = \sqrt{2.5/10} = 0.5$$

or $$V_{GS} = -2.5 \text{ V}$$

Now, $$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{30}{1000 + 500} \times 500$$

$$= 10 \text{ V}$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$10 \text{ V} = -2.5 \text{ V} + 2.5 \text{ mA} \times R_S$$

$$\therefore \quad R_S = \frac{10 \text{ V} + 2.5 \text{ V}}{2.5 \text{ mA}} = \frac{12.5 \text{ V}}{2.5 \text{ mA}}$$

$$= \mathbf{5\ k\Omega}$$

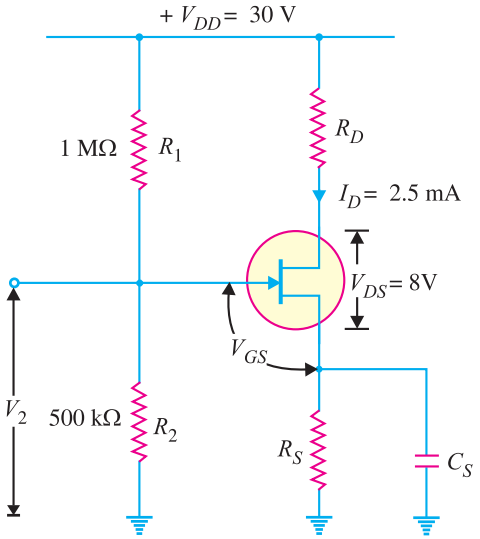


Fig. 19.28

19.20 JFET Connections

There are three leads in a *JFET viz.*, source, gate and drain terminals. However, when *JFET* is to be connected in a circuit, we require four terminals ; two for the input and two for the output. This difficulty is overcome by making one terminal of the *JFET* common to both input and output terminals. Accordingly, a *JFET* can be connected in a circuit in the following three ways :

(*i*) Common source connection **(*ii*)** Common gate connection

(*iii*) Common drain connection

The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and a moderate output impedance. However, the circuit produces a phase reversal *i.e.*, output signal is 180° out of phase with the input signal. Fig. 19.29 shows a common source *n*-channel *JFET* amplifier. Note that source terminal is common to both input and output.

Note. A common source *JFET* amplifier is the *JFET* equivalent of common emitter amplifier. Both amplifiers have a 180° phase shift from input to output. Although the two amplifiers serve the same basic purpose, the means by which they operate are quite different.

19.21 Practical JFET Amplifier

It is important to note that a *JFET* can accomplish faithful amplification only if proper associated circuitry is used. Fig. 19.29 shows the practical circuit of a *JFET*. The gate resistor R_G serves two purposes. It keeps the gate at approximately 0 V dc (Q gate current is nearly zero) and its large value (usually several megaohms) prevents loading of the a.c. signal source. The bias voltage is created by the drop across R_S. The bypass capacitor C_S bypasses the a.c. signal and thus keeps the source of the *JFET* effectively at a.c. ground. The coupling capacitor C_{in} couples the signal to the input of *JFET* amplifier.

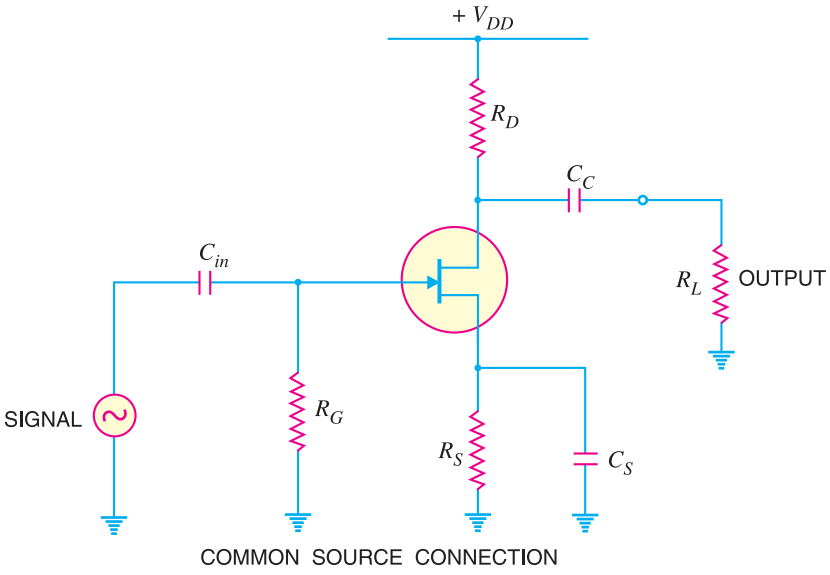


Fig. 19.29

19.22 D.C. and A.C. Equivalent Circuits of JFET

Like in a transistor amplifier, both d.c. and a.c. conditions prevail in a *JFET* amplifier. The d.c. sources set up d.c. currents and voltages whereas the a.c. source (*i.e.* signal) produces fluctuations in the *JFET* currents and voltages. Therefore, a simple way to analyse the action of a *JFET* amplifier is to split the circuit into two parts *viz.* *d.c. equivalent circuit* and *a.c. equivalent circuit.* The d.c. equivalent circuit will determine the operating point (d.c. bias levels) for the circuit while a.c. equivalent circuit determines the output voltage and hence voltage gain of the circuit.

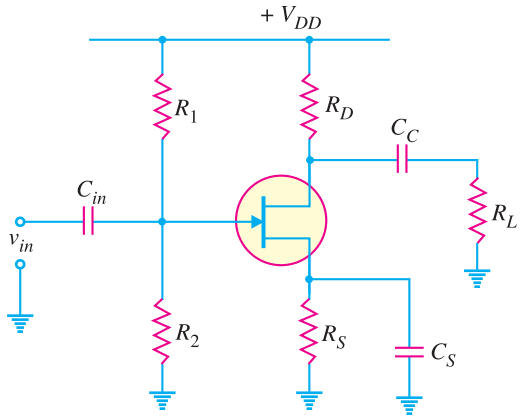


Fig. 19.30

We shall split the *JFET* amplifier shown in Fig. 19.30 into d.c. and a.c. equivalent circuits. Note that biasing is provided by voltage-divider circuit.

1. **D. C. equivalent circuit.** In the d.c. equivalent circuit of a *JFET* amplifier, only d.c. conditions are considered *i.e.* it is presumed that no signal is applied. As direct current cannot

flow through a capacitor, *all the capacitors look like open circuits in the d.c. equivalent circuit.* It follows, therefore, that in order to draw the d.c. equivalent circuit, the following two steps are applied to the *JFET* amplifier circuit :

(*i*) Reduce all a.c. sources to zero.

(*ii*) Open all the capacitors.

Applying these two steps to the *JFET* amplifier circuit shown in Fig. 19.30, we get the d.c. equivalent circuit shown in Fig. 19.31. We can easily calculate the d.c. currents and voltages from this circuit.

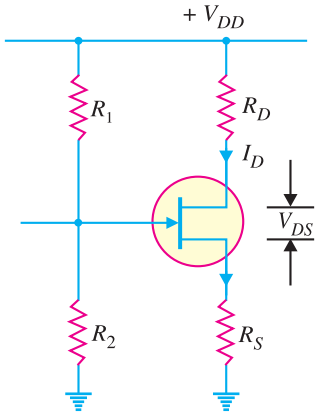


Fig. 19.31

2. A. C. equivalent circuit. In the a.c. equivalent circuit of a *JFET* amplifier, only a.c. conditions are to be considered. Obviously, the d.c. voltage is not important for such a circuit and may be considered zero. The capacitors are generally used to couple or bypass the a.c. signal. The designer intentionally selects capacitors that are large enough to appear as *short circuits* to the a.c. signal. It follows, therefore, that in order to draw the a.c. equivalent circuit, the following two steps are applied to the *JFET* amplifier circuit :

(*i*) Reduce all d.c. sources to zero (*i.e.* $V_{DD} = 0$).

(*ii*) Short all the capacitors.

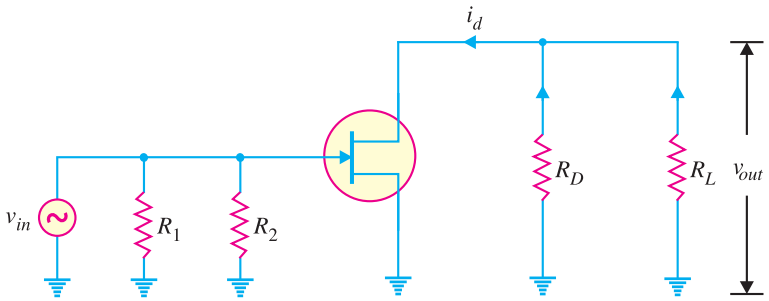


Fig. 19.32

Applying these two steps to the circuit shown in Fig. 19.30, we get the a.c. *equivalent circuit shown in Fig. 19.32. We can easily calculate the a.c. currents and voltages from this circuit.

19.23 D.C. Load Line Analysis

The operating point of a *JFET* amplifier can be determined graphically by drawing d.c. load line on the drain characteristics ($V_{DS} - I_D$ curves). This method is identical to that used for transistors.

The d.c. equivalent circuit of a *JFET* amplifier using voltage-divider bias is shown in Fig. 19.33 (*i*). It is clear that :

$$V_{DD} = V_{DS} + I_D (R_D + R_S)$$

or $$V_{DS} = V_{DD} - I_D (R_D + R_S) \quad \ldots (i)$$

* Note that one end of R_1 and R_2 is connected to one point (See Fig. 19.32) and the other end of R_1 and R_2 is connected to ground. Therefore, $R_1 \parallel R_2$. Similar is the case with R_D and R_L so that $R_D \parallel R_L$.

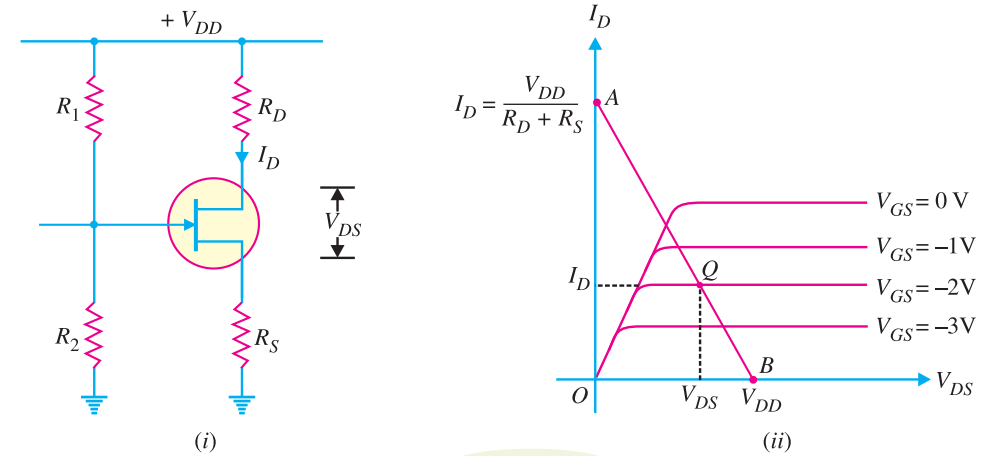


Fig. 19.33

As for a given circuit, V_{DD} and $(R_D + R_S)$ are constant, therefore, exp. (*i*) is a first degree equation and can be represented by a straight line on the drain characteristics. This is known as d.c. load line for *JFET* and determines the locus of I_D and V_{DS} (*i.e.* operating point) in the absence of the signal. The d.c. load line can be readily plotted by locating the *two end points* of the straight line.

(*i*) The value of V_{DS} will be maximum when $I_D = 0$. Therefore, by putting $I_D = 0$ in exp. (*i*) above, we get,

$$\text{Max. } V_{DS} = V_{DD}$$

This locates the first point B ($OB = V_{DD}$) of the d.c. load line on drain-source voltage axis.

(*ii*) The value of I_D will be maximum when $V_{DS} = 0$.

$$\therefore \quad \text{Max. } I_D = \frac{V_{DD}}{R_D + R_S}$$

This locates the second point A ($OA = V_{DD} / R_D + R_S$) of the d.c. load line on drain current axis.

By joining points A and B, d.c. load line AB is constructed [See Fig. 19.33 (*ii*)].

The operating point Q is located at the intersection of the d.c. load line and the drain curve which corresponds to V_{GS} provided by biasing. If we assume in Fig. 19.33 (*i*) that $V_{GS} = -2$V, then point Q is located at the intersection of the d.c. load line and the $V_{GS} = -2$V curve as shown in Fig. 19.33 (*ii*). The I_D and V_{DS} of Q point are marked on the graph.

Example 19.22. *Draw the d.c. load line for the JFET amplifier shown in Fig. 19.34 (i).*

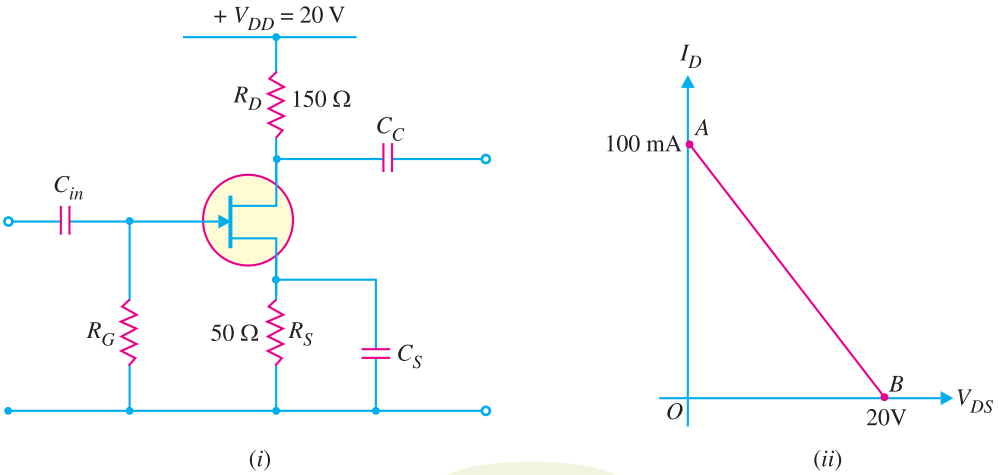


Fig. 19.34

Solution. To draw d.c. load line, we require two end points *viz.*, max V_{DS} and max. I_D points.

$$\text{Max. } V_{DS} = V_{DD} = 20\text{V}$$

This locates point B ($OB = 20$V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D + R_S} = \frac{20\text{V}}{(150 + 50)\ \Omega}$$

$$= \frac{20\text{V}}{200\Omega} = 100\text{ mA}$$

This locates point A ($OA = 100$ mA) of the d.c. load line. Joining A and B, d.c. load line AB is constructed as shown in Fig. 19.34 (*ii*).

Example 19.23. *Draw the d.c. load line for the JFET amplifier shown in Fig. 19.35 (i).*

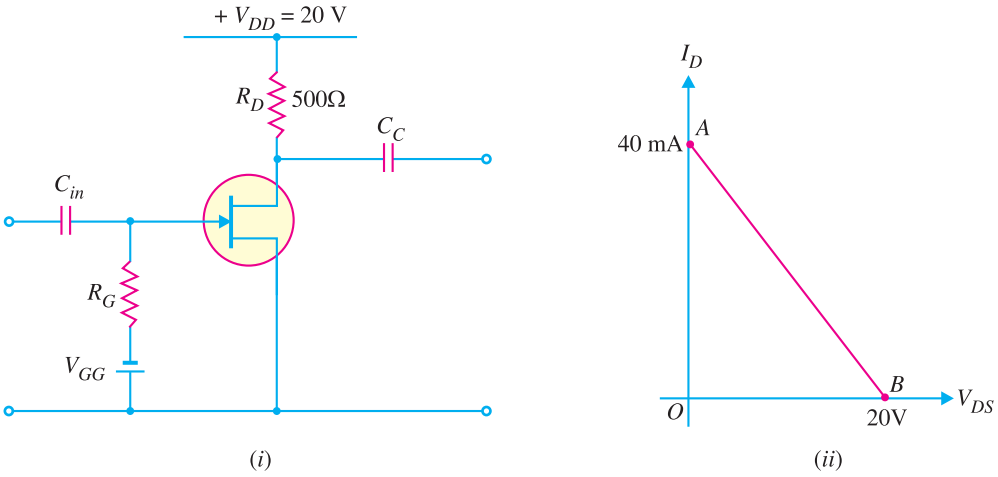


Fig. 19.35

Solution.

$$\text{Max. } V_{DS} = V_{DD} = 20\text{V}$$

This locates the point B ($OB = 20$V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D} = \frac{20\text{V}}{500\Omega} = 40\text{ mA}$$

This locates the point A ($OA = 40$ mA) of the d.c. load line.

Fig. 19.35 (*ii*) shows the d.c. load line AB.

19.24 Voltage Gain of JFET Amplifier

The a.c. equivalent circuit of *JFET* amplifier was developed in Art. 19.22 and is redrawn as Fig. 19.36 (*i*) for facility of reference. Note that $R_1 \parallel R_2$ and can be replaced by a single resistance R_T. Similarly, $R_D \parallel R_L$ and can be replaced by a single resistance R_{AC} (= total a.c. drain resistance). The a.c. equivalent circuit shown in Fig. 19.36 (*i*) then reduces to the one shown in Fig. 19.36 (*ii*).

We now find the expression for voltage gain of this amplifier. Referring to Fig. 19.36 (*ii*), output voltage (v_{out}) is given by ;

$$v_{out} = i_d R_{AC} \qquad \ldots (i)$$

Remember that we define g_m as :

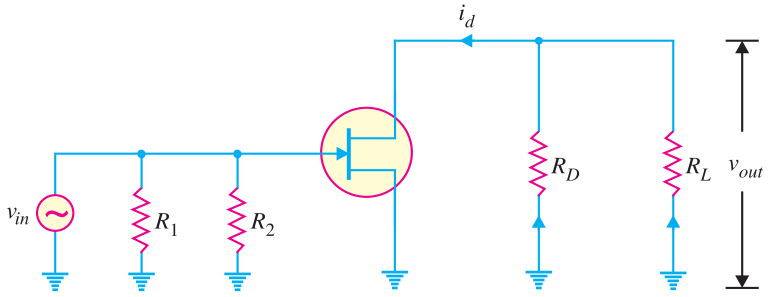


Fig. 19.36 (*i*)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

or $$g_m = \frac{i_d}{v_{gs}}$$

or $$i_d = g_m v_{gs}$$

Putting the value of i_d ($= g_m v_{gs}$) in eq. (*i*), we have,

$$v_{out} = g_m v_{gs} R_{AC}$$

Now $v_{in} = v_{gs}$ so that a.c. output voltage is

$$v_{out} = g_m v_{in} R_{AC}$$

or $$v_{out}/v_{in} = g_m R_{AC}$$

But v_{out}/v_{in} is the voltage gain (A_v) of the amplifier.

$\therefore$ Voltage gain, $A_v = g_m R_{AC}$ ... for loaded amplifier

$= g_m R_D$ ... for unloaded amplifier

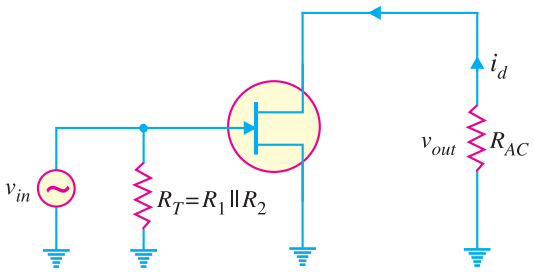


Fig. 19.36 (*ii*)

Example 19.24. *The JFET in the amplifier of Fig. 19.37 has a transconductance g_m = 1 mA/V. If the source resistance R_S is very small as compared to R_G, find the voltage gain of the amplifier.*

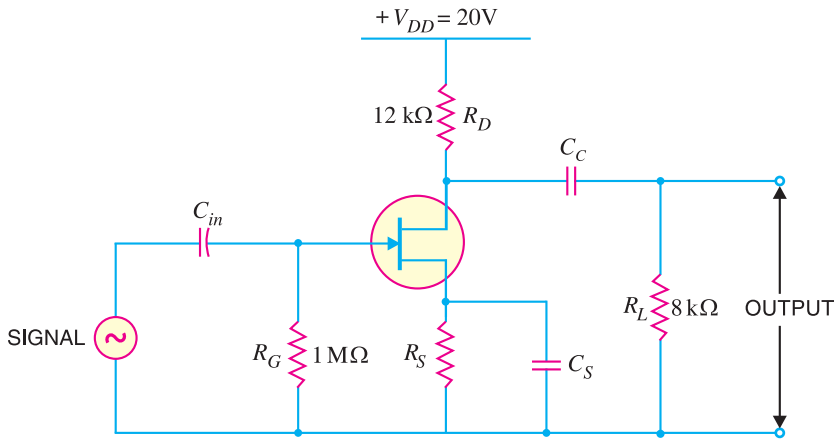


Fig. 19.37

Solution.

Transconductance of *JFET*, g_m = 1 mA/V

$= 1000\ \mu\text{ mho} = 1000 \times 10^{-6}\text{ mho}$

The total *ac* load (*i.e.* R_{AC}) in the drain circuit consists of the parallel combination of R_D and R_L *i.e.*

$$\text{Total a.c. load, } R_{AC} = R_D \parallel R_L$$

$$= 12\ \text{k}\Omega \parallel 8\ \text{k}\Omega = \frac{12 \times 8}{12 + 8} = 4.8\ \text{k}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = g_m \times R_{AC}$$

$$= (1000 \times 10^{-6}) \times (4.8 \times 10^3) = \mathbf{4.8}$$

Example 19.25. *The transconductance of a JFET used as a voltage amplifier is 3000 μmho and drain resistance is 10 kΩ. Calculate the voltage gain of the amplifier.*

Solution.

Transconductance of *JFET*, $g_m = 3000\ \mu\text{mho} = 3000 \times 10^{-6}\text{ mho}$

Drain resistance, $R_D = 10\ \text{k}\Omega = 10 \times 10^3\ \Omega$

$\therefore$ Voltage gain, $A_v = g_m R_D = (3000 \times 10^{-6})\ (10 \times 10^3) = \mathbf{30}$

Example 19.26. *What is the r.m.s. output voltage of the unloaded amplifier in Fig. 19.38? The I_{DSS} = 8 mA, $V_{GS\,(off)}$ = – 10V and I_D = 1.9 mA.*

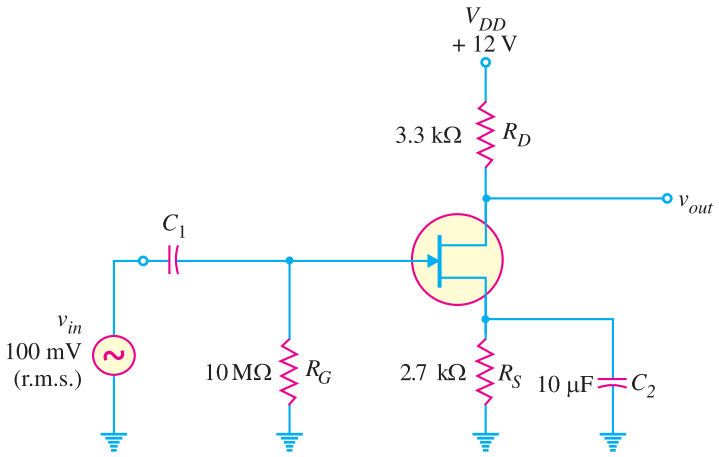


Fig. 19.38

Solution.

$$V_{GS} = -I_D R_S = -1.9\ \text{mA} \times 2.7 \times 10^3\ \Omega = -5.13\text{V}$$

$$g_{mo} = \frac{2\, I_{DSS}}{|V_{GS\,(off)}|} = \frac{2 \times 8\ \text{mA}}{10\ \text{V}} = 1.6 \times 10^{-3}\text{S}$$

$$\therefore \quad g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right) = 1.6 \times 10^{-3}\left(1 - \frac{-5.13\text{V}}{-10\text{V}}\right) = 779 \times 10^{-6}\ \text{S}$$

$$\text{Voltage gain, } A_v = g_m R_D = (779 \times 10^{-6})\ (3.3 \times 10^3) = 2.57$$

$\therefore$ Output voltage, $v_{out} = A_v\, v_{in} = 2.57 \times 100\ \text{mV} = \mathbf{257\ mV\ (r.m.s.)}$

Example 19.27. *If a 4.7 kΩ load resistor is a.c. coupled to the output of the amplifier in Fig. 19.38 above, what is the resulting r.m.s. output voltage?*

Solution. The value of g_m remains the same. However, the value of total a.c. drain resistance R_{AC} changes due to the connection of load R_L (= 4.7 kΩ).

$$\text{Total a.c. drain resistance, } R_{AC} = R_D \parallel R_L$$

$$= \frac{R_D R_L}{R_D + R_L} = \frac{(3.3\,k\Omega)(4.7\,k\Omega)}{3.3\,k\Omega + 4.7\,k\Omega} = 1.94\,k\Omega$$

$\therefore$ Voltage gain, $A_v = g_m R_{AC} = (779 \times 10^{-6})(1.94 \times 10^3) = 1.51$

Output voltage, $v_{out} = A_v v_{in} = 1.51 \times 100\,mV =$ **151 mV (r.m.s.)**

19.25 Voltage Gain of JFET Amplifier (*With Source Resistance R_S*)

Fig. 19.39 (*i*) shows the *JFET* amplifier with source resistor R_S unbypassed. This means that a.c. signal will not be bypassed by the capacitor C_S.

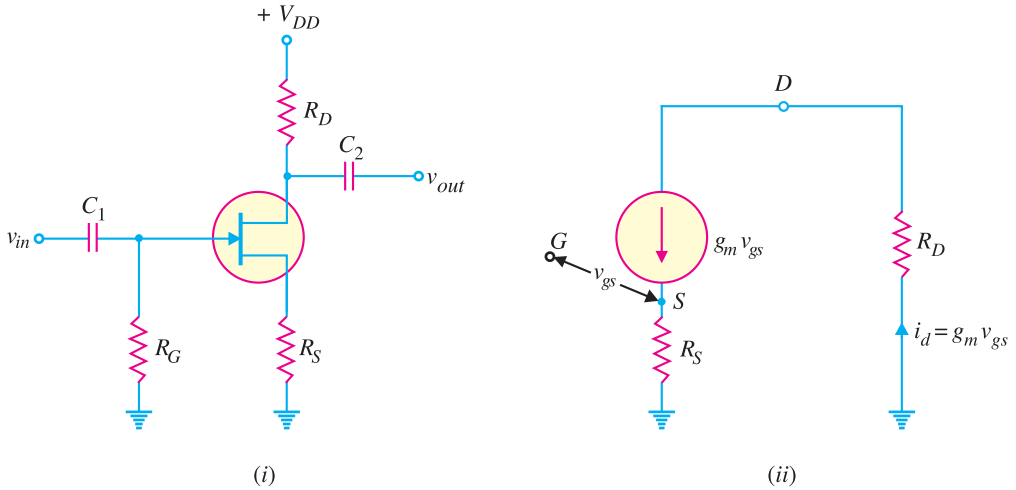


Fig. 19.39

Fig. 19.39 (*ii*) shows the simplified a.c. equivalent circuit of the *JFET* amplifier. Since $g_m = i_d/v_{gs}$, a current source $i_d = g_m v_{gs}$ appears between drain and source. Referring to Fig. 19.39 (*ii*),

$$v_{in} = v_{gs} + i_d R_S$$

$$v_{out} = i_d R_D$$

$\therefore$ Voltage gain, $A_v = \dfrac{v_{out}}{v_{in}} = \dfrac{i_d R_D}{v_{gs} + i_d R_S}$

$$= \frac{g_m v_{gs} R_D}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m v_{gs} R_D}{v_{gs}(1 + g_m R_S)} \qquad (\because\ i_d = g_m v_{gs})$$

$\therefore$ $A_v = \dfrac{g_m R_D}{1 + g_m R_S}$ ... for unloaded amplifier

$= \dfrac{g_m R_{AC}}{1 + g_m R_S}$ ... for loaded amplifier

Note that R_{AC} $(= R_D \parallel R_L)$ is the total a.c. drain resistance.

Example 19.28. *In a JFET amplifier, the source resistance R_S is unbypassed. Find the voltage gain of the amplifier. Given g_m = 4 mS; R_D = 1.5 kΩ and R_S = 560Ω.*

Solution.

Voltage gain, $A_v = \dfrac{g_m R_D}{1 + g_m R_S}$

Here $g_m = 4\,mS = 4 \times 10^{-3}\,S$; $R_D = 1.5\,k\Omega = 1.5 \times 10^3\,\Omega$; $R_S = 560\Omega$

$$\therefore \quad A_v = \frac{(4\times10^{-3})(1.5\times10^{3})}{1+(4\times10^{-3})(560)} = \frac{6}{1+2.24} = \mathbf{1.85}$$

If R_S is bypassed by a capacitor, then,

$$A_v = g_m R_D = (4 \times 10^{-3})(1.5 \times 10^{3}) = 6$$

Thus with unbypassed R_S, the gain = 1.85 whereas with R_S bypassed by a capacitor, the gain is 6. Therefore, voltage gain is reduced when R_S is unbypassed.

Example 19.29. *For the JFET amplifier circuit shown in Fig. 19.40, calculate the voltage gain with (i) R_S bypassed by a capacitor (ii) R_S unbypassed.*

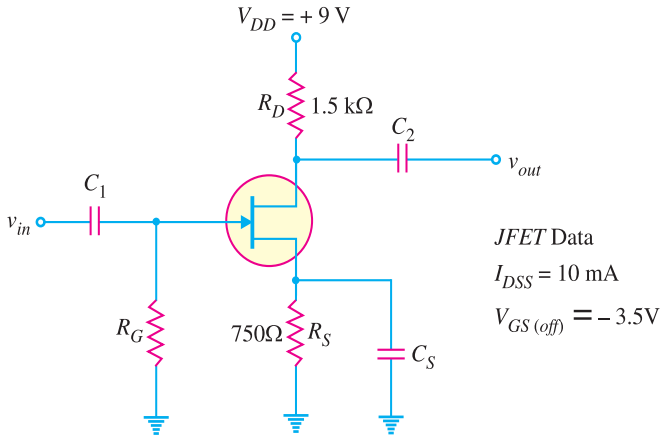


Fig. 19.40

Solution. From the d.c. bias analysis, we get, *I_D = 2.3 mA and V_{GS} = – 1.8V.

The value of g_m is given by;

$$g_m = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= \frac{2\times10}{3.5}\left(1-\frac{-1.8}{-3.5}\right) = (5.7\text{ mS})\,(0.486) = 2.77\text{ mS}$$

(*i*) The voltage gain with R_S bypassed is

$$A_v = g_m R_D = (2.77\text{ mS})\,(1.5\text{ k}\Omega) = \mathbf{4.155}$$

(*ii*) The voltage gain with R_S unbypassed is

$$A_v = \frac{g_m R_D}{1+g_m R_S} = \frac{4.155}{1+(2.77\text{ mS})\,(0.75\text{ k}\Omega)} = \mathbf{1.35}$$

19.26 JFET Applications

The high input impedance and low output impedance and low noise level make *JFET* far superior to the bipolar transistor. Some of the circuit applications of *JFET* are :

* $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS\,(off)}}\right]^2$ and $V_{GS} = -I_D R_S$

The unknown quantities V_{GS} and I_D can be found from these two equations.

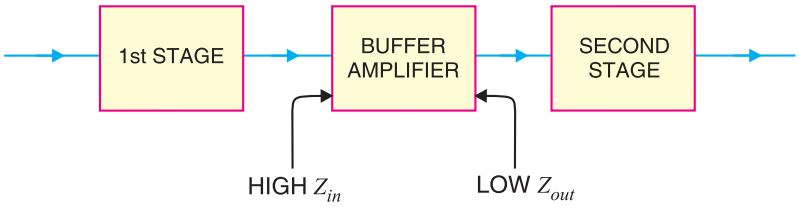


Fig. 19.41

(*i*) As a buffer amplifier. A buffer amplifier is a stage of amplification that isolates the preceding stage from the following stage. Because of the high input impedance and low output impedance, a *JFET* can act as an excellent buffer amplifier (See Fig. 19.41). The high input impedance of *JFET* means light loading of the preceding stage. This permits almost the entire output from first stage to appear at the buffer input. The low output impedance of *JFET* can drive heavy loads (or small load resistances). This ensures that all the output from the buffer reaches the input of the second stage.

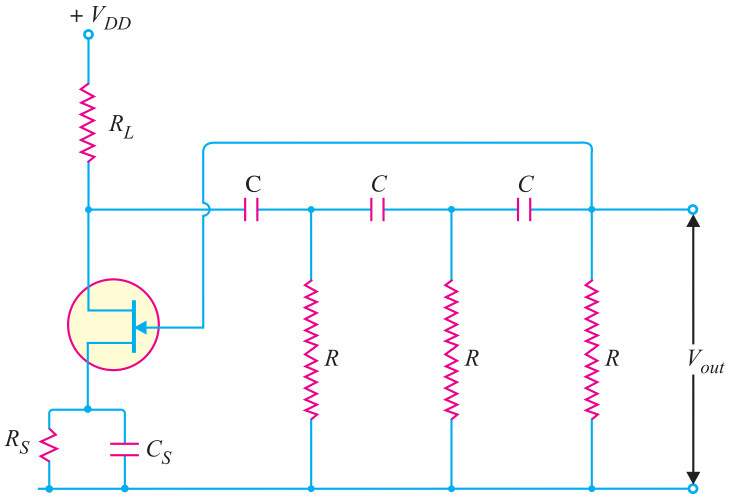


Fig. 19.42

(*ii*) Phase-shift oscillators. The oscillators discussed in chapter 14 will also work with *JFETs*. However, the high input impedance of *JFET* is especially valuable in phase-shift oscillators to minimise the loading effect. Fig. 19.42 shows the phase-shift oscillator using *n*-channel *JFET*.

(*iii*) As RF amplifier. In communication electronics, we have to use *JFET RF* amplifier in a receiver instead of *BJT* amplifier for the following reasons :

(*a*) The noise level of *JFET* is very low. The *JFET* will not generate significant amount of noise and is thus useful as an *RF* amplifier.

(*b*) The antenna of the receiver receives a very weak signal that has an extremely low amount of current. Since *JFET* is a voltage controlled device, it will well respond to low current signal provided by the antenna.

19.27 Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device *i.e.* it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (*i.e.* decrease the *conductivity of the channel) from its zero-bias size. This type of operation is referred to as **depletion-mode operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) *i.e.* it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

A field effect transistor (FET) that can be operated in the enhancement-mode is called a ***MOSFET.***

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

19.28 Types of MOSFETs

There are two basic types of *MOSFETs viz.*

1. Depletion-type *MOSFET* or ***D-MOSFET.*** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET*.
2. Enhancement-type *MOSFET* or ***E-MOSFET.*** The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET*.

1. D-MOSFET. Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(*i*) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons (Q it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).

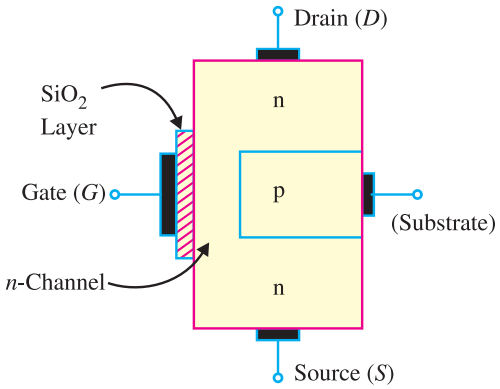
(*ii*) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET.*

(*iii*) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals *viz source* (*S*), *gate* (*G*) and *drain* (*D*).

(*iv*) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

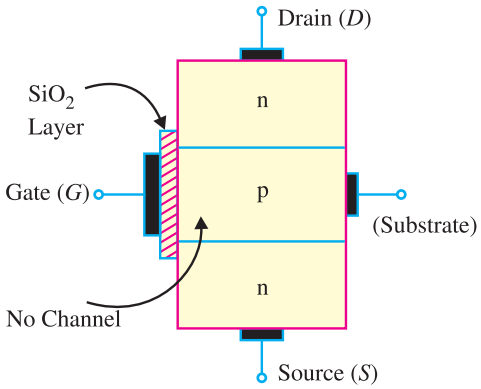
* With the decrease in channel width, the X-sectional area of the channel decreases and hence its resistance increases. This means that conductivity of the channel will decrease. Reverse happens if channel width increases.

** With gate reverse biased, the channel is depleted (*i.e.* emptied) of charge carriers (free electrons for *n*-channel and holes for *p*-channel) and hence the name depletion-mode. Note that depletion means decrease. In this mode of operation, conductivity decreases from the zero-bias level.



n-Channel D-MOSFET

Fig. 19.43



n-Channel E-MOSFET

Fig. 19.44

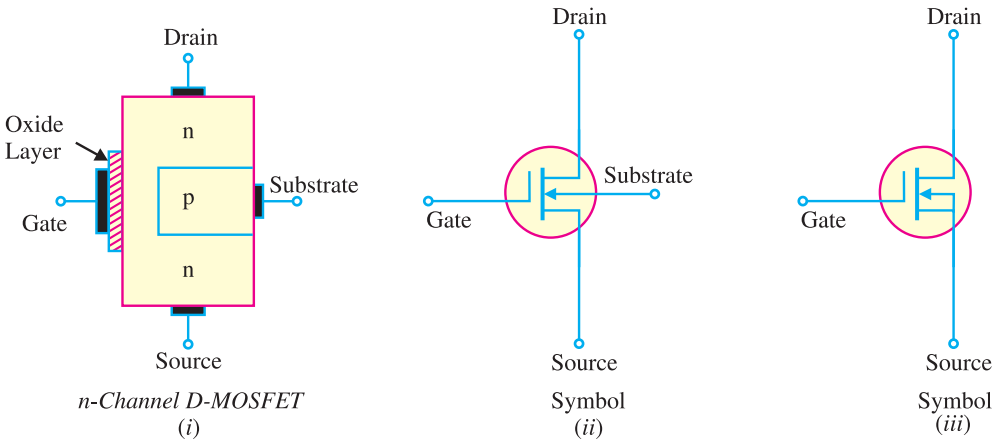
2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel *E-MOSFET*. Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.

Why the name MOSFET ? The reader may wonder why is the device called *MOSFET?* The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a *metal oxide semiconductor* and hence the name *MOSFET*. Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET).* However, this term is rarely used in place of the term *MOSFET*.

19.29 Symbols for D-MOSFET

There are two types of *D-MOSFETs viz* (*i*) *n*-channel *D-MOSFET* and (*ii*) *p*-channel *D-MOSFET*.

***(i)* n-channel D-MOSFET.** Fig. 19.45 (*i*) shows the various parts of *n*-channel *D-MOSFET*. The *p*-type substrate constricts the channel between the source and drain so that only a small passage



n-Channel D-MOSFET (*i*)

Symbol (*ii*)

Symbol (*iii*)

Fig. 19.45

remains at the left side. Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel. The symbol for *n*-channel *D-MOSFET* is shown in Fig. 19.45 (*ii*). The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel. The drain lead comes out of the top of the channel and the source lead connects to the bottom. The arrow is on the substrate and points to the *n*-material, therefore we have *n*-channel *D-MOSFET*. It is a usual practice to connect the substrate to source internally as shown in Fig. 19.45 (*iii*). This gives rise to a three-terminal device.

(*ii*) *p*-channel D-MOSFET. Fig. 19.46 (*i*) shows the various parts of *p*-channel *D-MOSFET*. The *n*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel. The symbol for *p*-channel *D-MOSFET* is shown in Fig. 19.46 (*ii*). It is a usual practice to connect the substrate to source internally. This results in a three-terminal device whose schematic symbol is shown in Fig. 19.46 (*iii*).

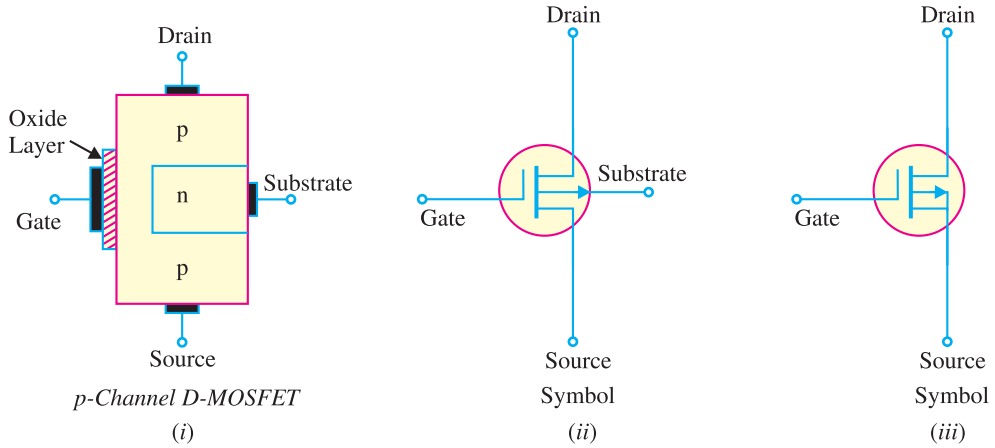


Fig. 19.46

19.30 Circuit Operation of D-MOSFET

Fig. 19.47 (*i*) shows the circuit of *n*-channel *D-MOSFET*. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called *depletion mode* whereas positive-gate operation is known as *enhancement mode.*

(*i*) Depletion mode. Fig. 19.47 (*i*) shows depletion-mode operation of *n*-channel *D-MOSFET*. Since gate is negative, it means electrons are on the gate as shown is Fig. 19.47 (*ii*). These electrons *repel the free electrons in the *n*-channel, leaving a layer of positive ions in a part of the channel as shown in Fig. 19.47 (*ii*). In other words, we have depleted (*i.e.* emptied) the *n*-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the *n*-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the *n*-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of *D-MOSFET* is similar to *JFET*. Because the action with negative gate depends upon depleting (*i.e.* emptying) the channel of free electrons, the negative-gate operation is called *depletion mode.*

* If one plate of the capacitor is negatively charged, it induces positive charge on the other plate.

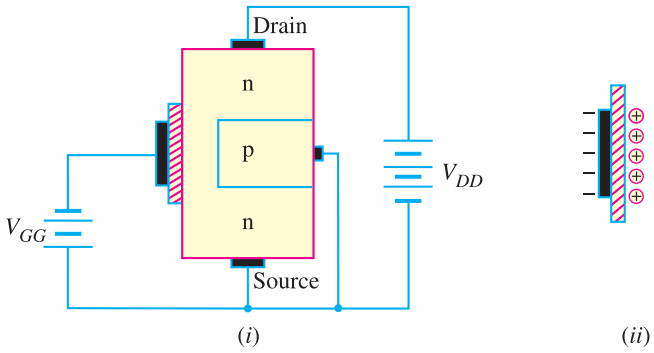


Fig. 19.47

(*ii*) Enhancement mode. Fig. 19.48 (*i*) shows enhancement-mode operation of *n*-channel *D-MOSFET*. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the *n*-channel as shown in Fig. 19.48 (*ii*). These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage *enhances* or *increases* the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between *D-MOSFET* and *JFET* is that we can apply positive gate voltage to *D-MOSFET* and still have essentially *zero current. Because the action with a positive gate depends upon *enhancing* the conductivity of the channel, the positive gate operation is called *enhancement mode.*

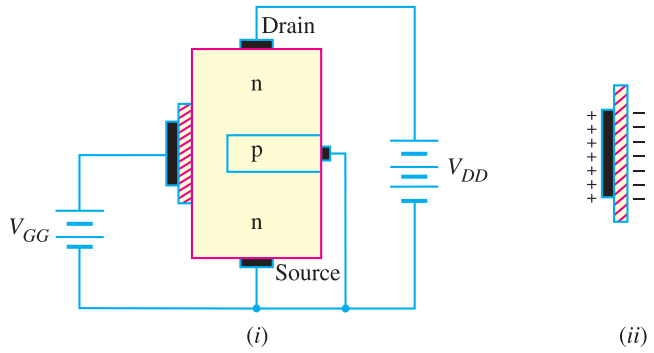


Fig. 19.48

The following points may be noted about *D-MOSFET* operation :

(*i*) In a *D-MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(*ii*) The gate of *JFET* behaves as a reverse-biased diode whereas the gate of a *D-MOSFET* acts like a capacitor. For this reason, it is possible to operate *D-MOSFET* with positive or negative gate voltage.

(*iii*) As the gate of *D-MOSFET* forms a capacitor, therefore, negligible gate current flows whether

* Note that gate of *JFET* is always reverse biased for proper operation. However, in a *MOSFET*, because of the insulating layer, a negligible gate current flows whether we apply negative or positive voltage to gate.

positive or negative voltage is applied to the gate. For this reason, the input impedance of *D-MOSFET* is very high, ranging from 10,000 MΩ to 10,000,00 MΩ.

(iv) The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the *D-MOSFET* has, therefore, a very low input capacitance. This characteristic makes the *D-MOSFET* useful in high-frequency applications.

19.31 D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*. The behaviour of this device can be beautifully explained with the help of this curve as under :

(i) The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted *i.e.* $V_{GS} = 0$.

(ii) As V_{GS} goes *negative*, I_D decreases below the value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS\,(off)}$ just as with *JFET*.

(iii) When V_{GS} is *positive*, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*.

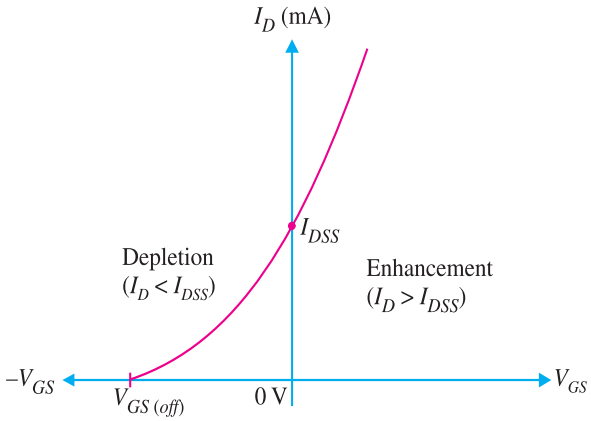


Fig. 19.49

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation *viz.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Example 19.30. *For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 8V.*

(*i*) *Is this an n-channel or a p-channel ?*

(*ii*) *Calculate I_D at V_{GS} = – 3V.*

(*iii*) *Calculate I_D at V_{GS} = + 3V.*

Solution.

(i) The device has a negative $V_{GS\,(off)}$. Therefore, it is ***n*-channel *D-MOSFET***.

(ii)
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{-3}{-8}\right)^2 = \mathbf{3.91\text{ mA}}$$

(iii)
$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$
$$= 10\text{ mA}\left(1-\frac{+3V}{-8V}\right)^2 = \mathbf{18.9\text{ mA}}$$

Example 19.31. *A D-MOSFET has parameters of $V_{GS\,(off)} = -6V$ and $I_{DSS} = 1$ mA. How will you plot the transconductance curve for the device ?*

Solution. When $V_{GS} = 0$ V, $I_D = I_{DSS} = 1$ mA and when $V_{GS} = V_{GS\,(off)}$, $I_D = 0$A. This locates two points *viz* I_{DSS} and $V_{GS\,(off)}$ on the transconductance curve. We can locate more points of the curve by *changing V_{GS} values.

When $V_{GS} = -3$V ; $I_D = 1\text{ mA}\left(1-\frac{-3V}{-6V}\right)^2 = 0.25$ mA

When $V_{GS} = -1$V ; $I_D = 1\text{ mA}\left(1-\frac{-1V}{-6V}\right)^2 = 0.694$ mA

When $V_{GS} = +1$V ; $I_D = 1\text{ mA}\left(1-\frac{+1V}{-6V}\right)^2 = 1.36$ mA

When $V_{GS} = +3$V ; $I_D = 1\text{ mA}\left(1-\frac{+3V}{-6V}\right)^2 = 2.25$ mA

Thus we have a number of $V_{GS} - I_D$ readings so that transconductance curve for the device can be readily plotted.

19.32 Transconductance and Input Impedance of D-MOSFET

These are important parameters of a *D-MOSFET* and a brief discussion on them is desirable.

(i) D-MOSFET Transconductance (g_m). The value of g_m is found for a *D-MOSFET* in the same way that it is for the *JFET i.e.*

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

(ii) D-MOSFET Input Impedance. The gate impedance of a *D-MOSFET* is extremely high. For example, a typical *D-MOSFET* may have a maximum gate current of 10 pA when $V_{GS} = 35$V.

$$\therefore \quad \text{Input impedance} = \frac{35\text{ V}}{10\text{ pA}} = \frac{35\text{V}}{10\times10^{-12}\text{ A}} = 3.5\times10^{12}\Omega$$

With an input impedance in this range, *D-MOSFET* would present virtually no load to a source circuit.

19.33 D-MOSFET Biasing

The following methods may be used for *D-MOSFET* biasing :

(i) Gate bias **(ii)** Self-bias

(iii) Voltage-divider bias **(iv)** Zero bias

The first three methods are exactly the same as those used for *JFET*s and are not discussed here. However, the last method of zero-bias is widely used in *D-MOSFET* circuits.

Zero bias. Since a *D-MOSFET* can be operated with either positive or negative values of V_{GS}, we can set its Q-point at $V_{GS} = 0$V as shown in Fig. 19.50. Then an input a.c. signal to the gate can produce variations above and below the Q-point.

* We can only change V_{GS} because the values of I_{DSS} and $V_{GS\,(off)}$ are constant for a given *D-MOSFET*.

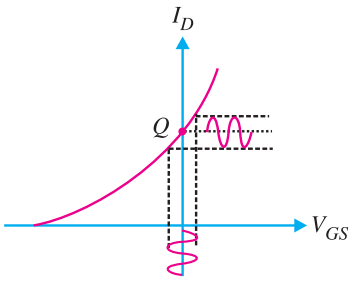


Fig. 19.50

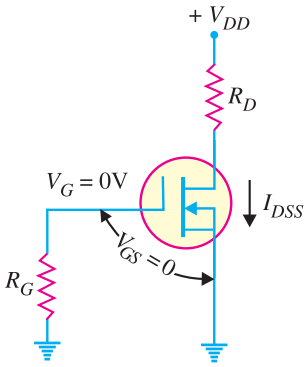


Fig. 19.51

We can use the simple circuit of Fig. 19.51 to provide zero bias. This circuit has $V_{GS} = 0$V and $I_D = I_{DSS}$. We can find V_{DS} as under :

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

Note that for the *D-MOSFET* zero bias circuit, the source resistor (R_S) is not necessary. With no source resistor, the value of V_S is 0V. This gives us a value of $V_{GS} = 0$V. This biases the circuit at $I_D = I_{DSS}$ and $V_{GS} = 0$V. For mid-point biasing, the value of R_D is so selected that $V_{DS} = V_{DD}/2$.

Example 19.32. *Determine the drain-to-source voltage (V_{DS}) in the circuit shown in Fig. 19.51 above if $V_{DD} = +18V$ and $R_D = 620\Omega$. The MOSFET data sheet gives $V_{GS(off)} = -8V$ and $I_{DSS} = 12$ mA.*

Solution. Since $I_D = I_{DSS} = 12$ mA, the V_{DS} is given by;

$$V_{DS} = V_{DD} - I_{DSS} R_D$$
$$= 18\text{V} - (12\text{ mA})\,(0.62\text{ k}\Omega) = \mathbf{10.6V}$$

19.34 Common-Source D-MOSFET Amplifier

Fig. 19.52 shows a common-source amplifier using *n*-channel *D-MOSFET*. Since the source terminal is common to the input and output terminals, the circuit is called *common-source amplifier. The circuit is zero biased with an a.c. source coupled to the gate through the coupling capacitor C_1. The gate is at approximately 0V d.c. and the source terminal is grounded, thus making $V_{GS} = 0$V.

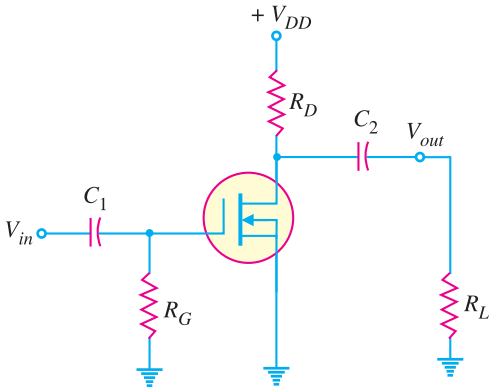


Fig. 19.52

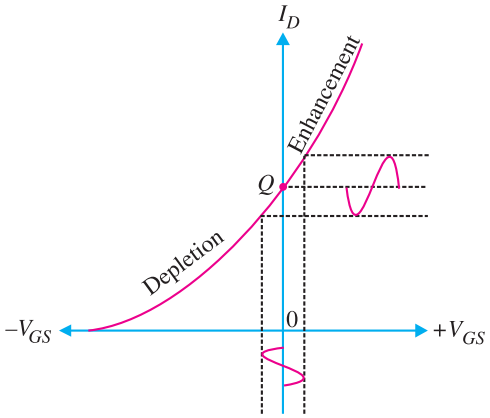


Fig. 19.53

* It is comparable to common-emitter transistor amplifier.

Operation. The input signal (V_{in}) is capacitively coupled to the gate terminal. In the absence of the signal, d.c. value of $V_{GS} = 0$V. When signal (V_{in}) is applied, V_{gs} swings above and below its zero value (Q d.c. value of $V_{GS} = 0$V), producing a swing in drain current I_d.

(i) A small change in gate voltage produces a large change in drain current as in a *JFET*. This fact makes *MOSFET* capable of raising the strength of a weak signal; thus acting as an amplifier.

(ii) During the positive half-cycle of the signal, the positive voltage on the gate increases and produces the enhancement-mode. This increases the channel conductivity and hence the drain current.

(iii) During the negative half-cycle of the signal, the positive voltage on the gate decreases and produces depletion-mode. This decreases the conductivity and hence the drain current.

The result of above action is that a small change in gate voltage produces a large change in the drain current. This large variation in drain current produces a large a.c. output voltage across drain resistance R_D. In this way, *D-MOSFET* acts as an amplifier. Fig. 19.53 shows the amplifying action of *D-MOSFET* on transconductance curve.

Voltage gain. The a.c. analysis of *D-MOSFET* is similar to that of the *JFET*. Therefore, voltage gain expressions derived for *JFET* are also applicable to *D-MOSFET*.

$$\text{Voltage gain, } A_v = g_m R_D \quad \text{... for unloaded } D\text{-}MOSFET \text{ amplifier}$$
$$= g_m R_{AC} \quad \text{... for loaded } D\text{-}MOSFET \text{ amplifier}$$

Note the total a.c. drain resistance $R_{AC} = R_D \,||\, R_L$.

Example 19.33. *The D-MOSFET used in the amplifier of Fig. 19.54 has an I_{DSS} = 12 mA and g_m = 3.2 mS. Determine (i) d.c. drain-to-source voltage V_{DS} and (ii) a.c. output voltage. Given v_{in} = 500 mV.*

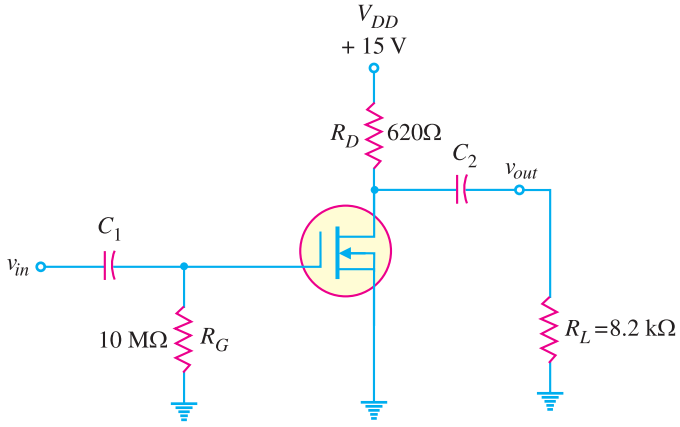


Fig. 19.54

Solution.

(i) Since the amplifier is zero biased, $I_D = I_{DSS} = 12$ mA.

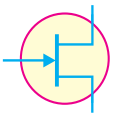
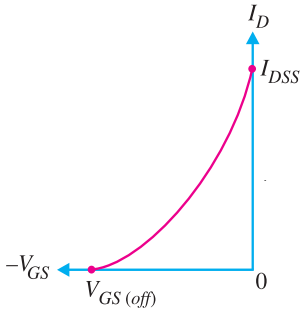
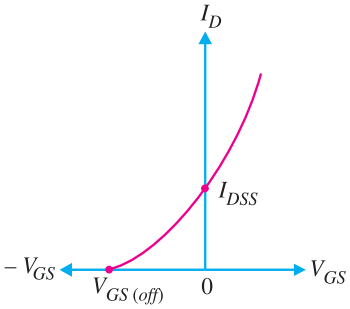
$$\therefore \quad V_{DS} = V_{DD} - I_{DSS} R_D$$
$$= 15\text{V} - (12\text{ mA})\,(0.62\text{ k}\Omega) = \mathbf{7.56V}$$

(ii) Total a.c. drain resistance R_{AC} of the circuit is

$$R_{AC} = R_D \,||\, R_L = 620\Omega \,||\, 8.2\text{ k}\Omega = 576\Omega$$
$$\therefore \quad v_{out} = A_v \times v_{in} = (g_m R_{AC})\,(v_{in})$$
$$= (3.2 \times 10^{-3}\ S \times 576\ \Omega)\,(500\text{ mV}) = \mathbf{922\ mV}$$

19.35 D-MOSFETs Versus JFETs

Table below summarises many of the characteristics of *JFET*s and *D-MOSFET*s.

Devices:	*JFETs*	*D-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion only	Depletion and enhancement
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias	Gate bias Self bias Voltage-divider bias Zero bias
Advantages:	Extremely high input impedance.	Higher input impedance than a comparable *JFET*. Can operate in both modes (depletion and enhancement).
Disadvantages:	Bias instability. Can operate only in the depletion mode.	Bias instability. More sensitive to changes in temperature than the *JFET*.

19.36 E-MOSFET

Two things are worth noting about *E-MOSFET*. First, *E-MOSFET* operates *only* in the enhancement mode and has no depletion mode. Secondly, the *E-MOSFET* has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig. 19.55 (*i*)]. It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the *E-MOSFET* is called *Threshold voltage* [$V_{GS\,(th)}$]. The *n*-channel device requires positive V_{GS} ($\geq V_{GS\,(th)}$) and the *p*-channel device requires negative V_{GS} ($\geqslant V_{GS\,(th)}$).

Operation. Fig. 19.55 (*i*) shows the circuit of *n*-channel *E-MOSFET*. The circuit action is as under :

(*i*) When $V_{GS} = 0$V [See Fig. 19.55(*i*)], there is no channel connecting the source and drain. The *p* substrate has only a few thermally produced free electrons (minority carriers) so that drain current is essentially zero. For this reason, *E-MOSFET* is normally *OFF* when $V_{GS} = 0$ V. Note that this behaviour of *E-MOSFET* is quite different from *JFET* or *D-MOSFET*.

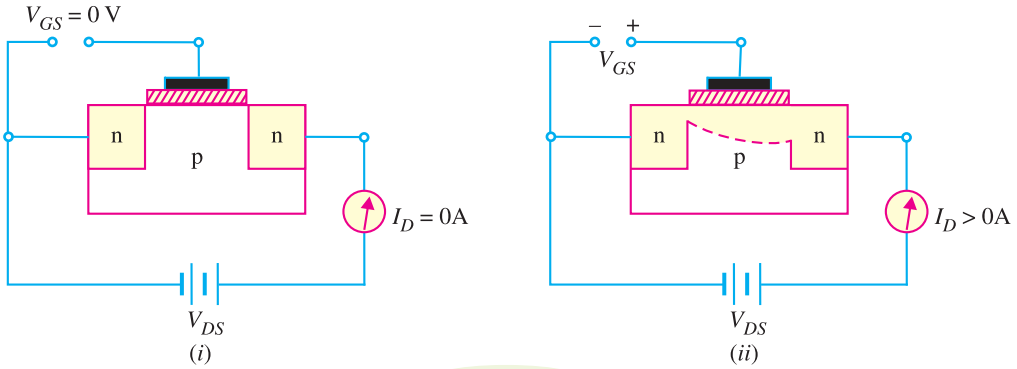


Fig. 19.55

(ii) When gate is made positive (*i.e.* V_{GS} is positive) as shown in Fig. 19.55 (*ii*), it attracts free electrons into th *p* region. The free electrons combine with the holes next to the SiO_2 layer. If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain. The effect is the same as creating a thin layer of *n*-type material (*i.e.* inducing a thin *n*-channel) adjacent to the SiO_2 layer. Thus the *E-MOSFET* is turned *ON* and drain current I_D starts flowing form the source to the drain.

The minimum value of V_{GS} that turns the E-MOSFET ON is called ***threshold voltage*** $[V_{GS\,(th)}]$.

(iii) When V_{GS} is less than $V_{GS\,(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS\,(th)}$, the *E-MOSFET* is turned *ON* and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS\,(th)}$, if the value of V_{GS} is *increased*, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases [not less than $V_{GS\,(th)}$], the channel becomes narrower and I_D will decrease. This fact is revealed by the transconductance curve of *n*-channel *E-MOSFET* shown in Fig. 19.56. As you can see, $I_D = 0$ when $V_{GS} = 0$. Therefore, the value of I_{DSS} for the *E-MOSFET* is zero. Note also that there is no drain current until V_{GS} reaches $V_{GS\,(th)}$.

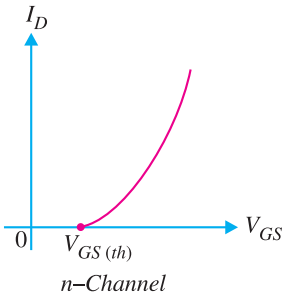


Fig. 19.56

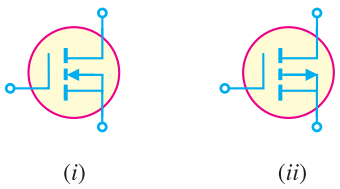


Fig. 19.57

Schematic Symbols. Fig. 19.57 (*i*) shows the schematic symbols for *n*-channel *E-MOSFET* whereas Fig. 19.57 (*ii*) shows the schematic symbol for *p*-channel *E-MOSFET.* When $V_{GS} = 0$, the *E-MOSFET* is *OFF* because there is no conducting channel between source and drain. The broken channel line in the symbols indicates the normally *OFF* condition.

Equation for Transconductance Curve. Fig. 19.58 shows the transconductance curve for *n*-channel *E-MOSFET*. Note that this curve is different from the transconductance curve for *n*-channel *JFET* or *n*-channel *D-MOSFET*. It is because it starts at $V_{GS\,(th)}$ rather than $V_{GS\,(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the *E-MOSFET* transconductance curve (for $V_{GS} > V_{GS\,(th)}$) is

$$I_D = K(V_{GS} - V_{GS\,(th)})^2$$

The constant K depends on the particular *E-MOSFET* and its value is determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

Any data sheet for an *E-MOSFET* will include the current $I_{D(on)}$ and the voltage $V_{GS\,(on)}$ for one point well above the threshold voltage as shown in Fig. 19.58.

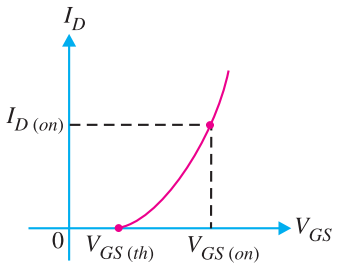


Fig. 19.58

Example 19.34. *The data sheet for an E-MOSFET gives $I_{D(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 1V. Determine the drain current for V_{GS} = 5V.*

Solution. Here $V_{GS\,(on)} = 10$ V.

$$I_D = K(V_{GS} - V_{GS\,(th)})^2 \quad \ldots (i)$$

Here $$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2} = \frac{500\text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17\text{ mA/V}^2$$

Putting the various values in eq. (*i*), we have,

$$I_D = 6.17\,(5\text{V} - 1\text{V})^2 = \mathbf{98.7\text{ mA}}$$

Example 19.35. *The data sheet for an E-MOSFET gives $I_{D\,(on)}$ = 3 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 3V. Determine the resulting value of K for the device. How will you plot the transconductance curve for this MOSFET ?*

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

Here $I_{D\,(on)} = 3$ mA ; $V_{GS\,(on)} = 10$V ; $V_{GS\,(th)} = 3$V

$$\therefore \quad K = \frac{3\text{ mA}}{(10\text{V} - 3\text{V})^2} = \frac{3\text{ mA}}{(7\text{V})^2} = \mathbf{0.061 \times 10^{-3}\ A/V^2}$$

Now $$I_D = K(V_{GS} - V_{GS\,(th)})^2$$

In order to plot the transconductance curve for the device, we shall determine a few points for the curve by changing the value of V_{GS} and noting the corresponding values of I_D.

For V_{GS} = 5V ; $I_D = 0.061 \times 10^{-3}\,(5\text{V} - 3\text{V})^2 = 0.244$ mA

For V_{GS} = 8V ; $I_D = 0.061 \times 10^{-3}\,(8\text{V} - 3\text{V})^2 = 1.525$ mA

For V_{GS} = 10V ; $I_D = 0.061 \times 10^{-3}\,(10\text{V} - 3\text{V})^2 = 3$ mA

For V_{GS} = 12V ; $I_D = 0.061 \times 10^{-3}\,(12\text{V} - 3\text{V})^2 = 4.94$ mA

Thus we can plot the transconductance curve for the *E-MOSFET* from these V_{GS}/I_D points.

19.37 E-MOSFET Biasing Circuits

One of the problems with *E-MOSFET* is the fact that many of the biasing circuits used for *JFETs* and *D-MOSFETs* cannot be used with this device. For example, *E-MOSFETs* must have V_{GS} greater than the threshold value ($V_{GS\,(th)}$) so that zero bias cannot be used. However, there are two popular methods for *E-MOSFET* biasing *viz.*

(*i*) Drain-feedback bias

(*ii*) Voltage-divider bias

(*i*) Drain-feedback bias. This method of *E-MOSFET* bias is equivalent to collector-feedback bias in transistors. Fig. 19.59 (*i*) shows the drain-feedback bias circuit for *n*-channel *E-MOSFET*. A

high resistance R_G is connected between the drain and the gate. Since the gate resistance is superhigh, no current will flow in the gate circuit (*i.e.* $I_G = 0$). Therefore, there will be no voltage drop across R_G. Since there is no voltage drop across R_G, the gate will be at the same potential as the drain. This fact is illustrated in the d.c. equivalent circuit of drain-feedback bias as in Fig. 19.59 (*ii*).

$$\therefore \qquad V_D = V_G \quad \text{and} \quad V_{DS} = V_{GS}$$

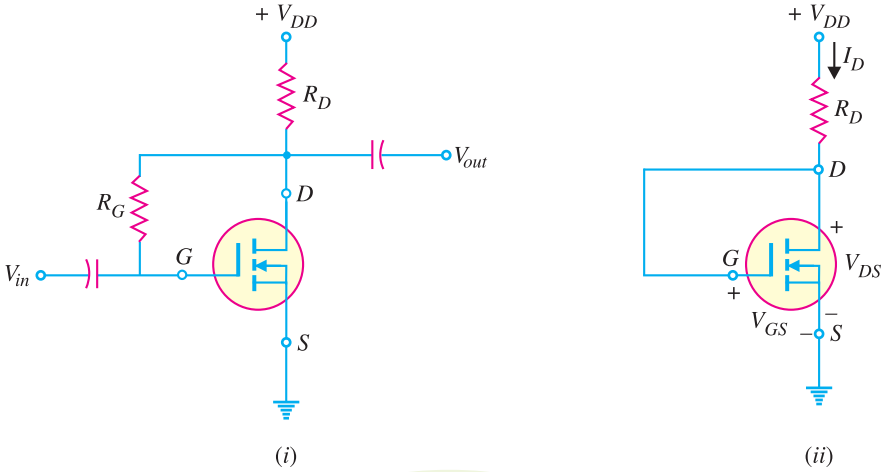


Fig. 19.59

The value of drain-source voltage V_{DS} for the drain-feedback circuit is

$$V_{DS} = V_{DD} - I_D R_D$$

Since $V_{DS} = V_{GS}$, $V_{GS} = V_{DD} - I_D R_D$

Since in this circuit $V_{DS} = V_{GS}$; $I_D = I_{D\,(on)}$.

Therefore, the *Q*-point of the circuit stands determined.

(*ii*) Voltage-divider Bias. Fig. 19.60 shows voltage divider biasing arrangement for *n*-channel *E-MOSFET*. Since $I_G = 0$, the analysis of the method is as follows :

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

and $$V_{DS} = V_{DD} - I_D R_D$$

where $$I_D = K (V_{GS} - V_{GS\,(th)})^2$$

Once I_D and V_{DS} are known, all the remaining quantities of the circuit such as V_D etc. can be determined.

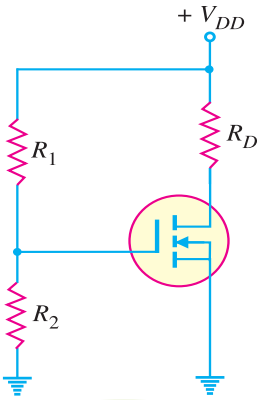


Fig. 19.60

Example 19.36. *Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Fig. 19.61. The data sheet for this particular MOSFET gives $I_{D\,(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 1V.*

Solution. Referring to the circuit shown in Fig. 19.61, we have,

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{24\text{V}}{(100 + 15)\,\text{k}\Omega} \times 15\,\text{k}\Omega = \mathbf{3.13V}$$

The value of K can be determined from the following equation :

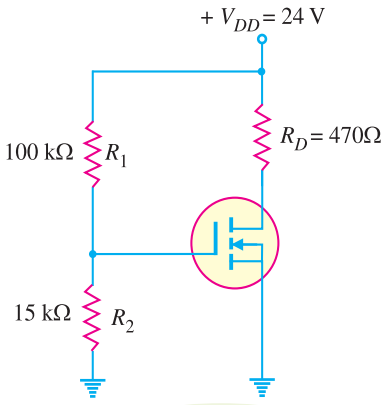


Fig. 19.61

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{500\text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17\text{ mA/V}^2 \quad [\because V_{GS\,(on)} = 10\text{V}]$$

$$\therefore \quad I_D = K\,(V_{GS} - V_{GS\,(th)})^2 = 6.17\text{ mA/V}^2\,(3.13\text{V} - 1\text{ V})^2 = 28\text{ mA}$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D = 24\text{V} - (28\text{ mA})\,(470\Omega) = \mathbf{10.8V}$$

Example 19.37. *Determine the values of I_D and V_{DS} for the circuit shown in Fig. 19.62. The data sheet for this particular MOSFET gives $I_{D\,(on)} = 10$ mA when $V_{GS} = V_{DS}$.*

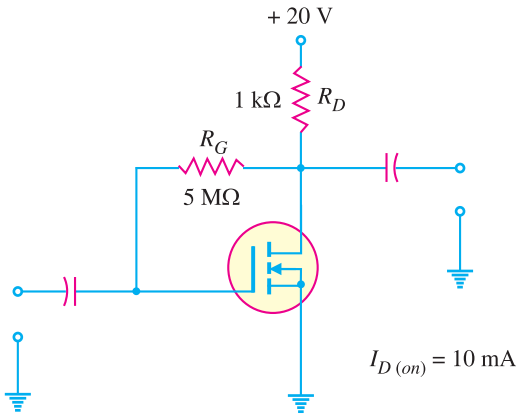


Fig. 19.62

Solution. Since in the drain-feedback circuit $V_{GS} = V_{DS}$,

$$\therefore \quad I_D = I_{D\,(on)} = \mathbf{10\text{ mA}}$$

The value of V_{DS} (and thus V_{GS}) is given by ;

$$V_{DS} = V_{DD} - I_D R_D$$

$$= 20\text{V} - (10\text{ mA})\,(1\text{ k}\Omega) = 20\text{V} - 10\text{V} = \mathbf{10V}$$

Example 19.38. *Determine the value of I_D for the circuit shown in Fig. 19.63. The data sheet for this particular MOSFET gives $I_{D\,(on)} = 10$ mA at $V_{GS} = 10$ V and $V_{GS\,(th)} = 1.5$ V.*

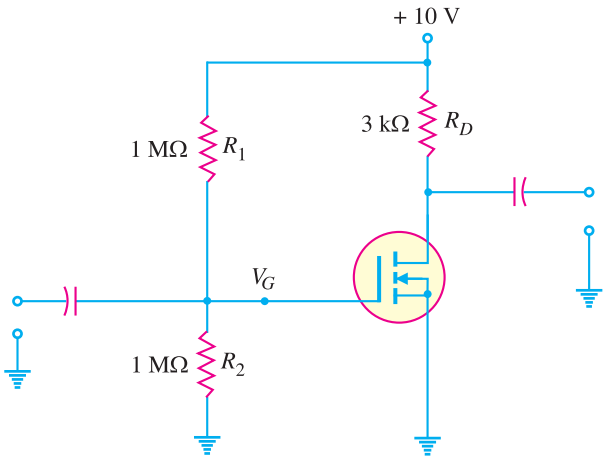


Fig. 19.63

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{10\text{ mA}}{(10\text{ V} - 1.5\text{V})^2} = 1.38 \times 10^{-1}\text{ mA/V}^2 \quad [\because\ V_{GS\,(on)} = 10\text{V}]$$

From the circuit, the source voltage is seen to be 0V. Therefore, $V_{GS} = V_G - V_S = V_G - 0 = V_G$. The value of V_G $(= V_{GS})$ is given by ;

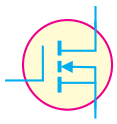
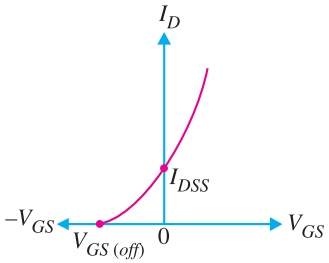
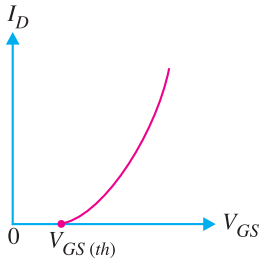
$$V_G \text{ (or } V_{GS}) = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{10\text{V}}{(1+1)\,\text{M}\Omega} \times 1\text{M}\Omega = 5\text{V}$$

$$\therefore \quad I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

$$= (1.38 \times 10^{-1}\text{ mA/V}^2)\,(5\text{V} - 1.5\text{V})^2 = \mathbf{1.69\ mA}$$

19.38 D-MOSFETs Versus E-MOSFETs

Table below summarises many of the characteristics of *D-MOSFETs* and *E-MOSFETs*

Devices:	*D-MOSFETs*	*E-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion and enhancement.	Enhancement only.
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias Zero bias	Gate bias Voltage-divider bias Drain-feedback bias

MULTIPLE-CHOICE QUESTIONS

1. A *JFET* has three terminals, namely .....
- (*i*) cathode, anode, grid
- (*ii*) emitter, base, collector
- (*iii*) source, gate, drain
- (*iv*) none of the above

2. A *JFET* is similar in operation to ..... valve.
- (*i*) diode (*ii*) pentode
- (*iii*) triode (*iv*) tetrode

3. A *JFET* is also called ..... transistor.
- (*i*) unipolar (*ii*) bipolar
- (*iii*) unijunction (*iv*) none of the above

4. A *JFET* is a ..... driven device.

(*i*) current
(*ii*) voltage
(*iii*) both current and voltage
(*iv*) none of the above

5. The gate of a *JFET* is ..... biased.
(*i*) reverse
(*ii*) forward
(*iii*) reverse as well as forward
(*iv*) none of the above

6. The input impedance of a *JFET* is ..... that of an ordinary transistor.
(*i*) equal to (*ii*) less than
(*iii*) more than (*iv*) none of the above

7. In a *p*-channel *JFET*, the charge carriers are .....
(*i*) electrons
(*ii*) holes
(*iii*) both electrons and holes
(*iv*) none of the above

8. When drain voltage equals the pinch-off voltage, then drain current ..... with the increase in drain voltage.
(*i*) decreases
(*ii*) increases
(*iii*) remains constant
(*iv*) none of the above

9. If the reverse bias on the gate of a *JFET* is increased, then width of the conducting channel .....
(*i*) is decreased
(*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

10. A *MOSFET* has ..... terminals.
(*i*) two (*ii*) five
(*iii*) four (*iv*) three

11. A *MOSFET* can be operated with .....
(*i*) negative gate voltage only
(*ii*) positive gate voltage only
(*iii*) positive as well as negative gate voltage
(*iv*) none of the above

12. A *JFET* has ..... power gain.
(*i*) small (*ii*) very high
(*iii*) very small (*iv*) none of the above

13. The input control parameter of a *JFET* is .....
(*i*) gate voltage (*ii*) source voltage
(*iii*) drain voltage (*iv*) gate current

14. A common base configuration of a *pnp* transistor is analogous to ..... of a *JFET*.
(*i*) common source configuration
(*ii*) common drain configuration
(*iii*) common gate configuration
(*iv*) none of the above

15. A *JFET* has high input impedance because .....
(*i*) it is made of semiconductor material
(*ii*) input is reverse biased
(*iii*) of impurity atoms
(*iv*) none of the above

16. In a *JFET*, when drain voltage is equal to pinch-off voltage, the depletion layers .....
(*i*) almost touch each other
(*ii*) have large gap
(*iii*) have moderate gap
(*iv*) none of the above

17. In a *JFET*, I_{DSS} is known as .....
(*i*) drain to source current
(*ii*) drain to source current with gate shorted
(*iii*) drain to source current with gate open
(*iv*) none of the above

18. The two important advantages of a *JFET* are .....
(*i*) high input impedance and square-law property
(*ii*) inexpensive and high output impedance
(*iii*) low input impedance and high output impedance
(*iv*) none of the above

19. ..... has the lowest noise-level.
(*i*) triode (*ii*) ordinary transistor
(*iii*) tetrode (*iv*) *JFET*

20. A *MOSFET* is sometimes called ..... *JFET*.
(*i*) many gate (*ii*) open gate
(*iii*) insulated gate (*iv*) shorted gate

21. Which of the following devices has the highest input impedance ?
(*i*) *JFET*

(*ii*) *MOSFET*
(*iii*) crystal diode
(*iv*) ordinary transistor

22. A *MOSFET* uses the electric field of a ..... to control the channel current.
(*i*) capacitor (*ii*) battery
(*iii*) generator (*iv*) none of the above

23. The pinch-off voltage in a *JFET* is analogous to ..... voltage in a vacuum tube.
(*i*) anode
(*ii*) cathode
(*iii*) grid cut off
(*iv*) none of the above

24. The formula for a.c. drain resistance of a *JFET* is .....
(*i*) $\frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}
(*ii*) $\frac{\Delta V_{GS}}{\Delta I_D}$ at constant V_{DS}
(*iii*) $\frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}
(*iv*) $\frac{\Delta I_D}{\Delta V_{DS}}$ at constant V_{GS}

25. In class *A* operation, the input circuit of a *JFET* is ..... biased.
(*i*) forward (*ii*) reverse
(*iii*) not (*iv*) none of the above

26. If the gate of a *JFET* is made less negative, the width of the conducting channel .....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

27. The pinch-off voltage of a *JFET* is about .....
(*i*) 5 V (*ii*) 0.6 V
(*iii*) 15 V (*iv*) 25 V

28. The input impedance of a *MOSFET* is of the order of .....
(*i*) Ω (*ii*) a few hundred Ω
(*iii*) k Ω (*iv*) several M Ω

29. The gate voltage in a *JFET* at which drain current becomes zero is called ..... voltage.
(*i*) saturation (*ii*) pinch-off
(*iii*) active (*iv*) cut-off

30. The drain current I_D in a *JFET* is given by .....
(*i*) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
(*ii*) $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$
(*iii*) $I_D = I_{DSS}\left(1 - \frac{V_P}{V_{GS}}\right)^2$
(*iv*) $I_D = I_{DSS}\left(1 + \frac{V_P}{V_{GS}}\right)^{1/2}$

31. In a *FET*, there are ..... *pn* junctions at the sides.
(*i*) three (*ii*) four
(*iii*) five (*iv*) two

32. The transconductance of a *JFET* ranges from .....
(*i*) 100 to 500 mA/V
(*ii*) 500 to 1000 mA/V
(*iii*) 0.5 to 30 mA/V
(*iv*) above 1000 mA/V

33. The source terminal of a *JFET* corresponds to ..... of a vacuum tube.
(*i*) plate (*ii*) cathode
(*iii*) grid (*iv*) none of the above

34. The output characteristics of a *JFET* closely resemble the output characteristics of a ..... valve.
(*i*) pentode (*ii*) tetrode
(*iii*) triode (*iv*) diode

35. If the cross-sectional area of the channel in *n*-channel *JFET* increases, the drain current .....
(*i*) is increased
(*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

36. The channel of a *JFET* is between the .....
(*i*) gate and drain
(*ii*) drain and source
(*iii*) gate and source
(*iv*) input and output

37. For $V_{GS} = 0$ V, the drain current becomes con-

stant when V_{DS} exceeds .....
(*i*) cut off (*ii*) V_{DD}
(*iii*) V_P (*iv*) 0 V

38. A certain *JFET* data sheet gives $V_{GS(off)} = -4$ V. The pinch-off voltage V_P is .....
(*i*) +4 V (*ii*) −4 V
(*iii*) dependent on V_{GS}
(*iv*) data insufficient

39. The constant-current region of a *JFET* lies between .....
(*i*) cut off and saturation
(*ii*) cut off and pinch-off
(*iii*) 0 and I_{DSS}
(*iv*) pinch-off and breakdown

40. At cut-off, the *JFET* channel is .....
(*i*) at its widest point
(*ii*) completely closed by the depletion region
(*iii*) extremely narrow
(*iv*) reverse biased

41. A *MOSFET* differs from a *JFET* mainly because .....
(*i*) of power rating
(*ii*) the *MOSFET* has two gates
(*iii*) the *JFET* has a *pn* junction
(*iv*) none of above

42. A certain *D-MOSFET* is biased at $V_{GS} = 0$V. Its data sheet specifies $I_{DSS} = 20$ mA and $V_{GS\,(off)} = -5$V. The value of the drain current is .....
(*i*) 20 mA (*ii*) 0 mA
(*iii*) 40 mA (*iv*) 10 mA

43. An *n*-channel *D-MOSFET* with a positive V_{GS} is operating in .....
(*i*) the depletion-mode
(*ii*) the enhancement-mode
(*iii*) cut off (*iv*) saturation

44. A certain *p*-channel E-MOSFET has a $V_{GS\,(th)} = -2$V. If $V_{GS} = 0$V, the drain current is .....
(*i*) 0 mA (*ii*) $I_{D\,(on)}$
(*iii*) maximum (*iv*) I_{DSS}

45. In a common-source *JFET* amplifier, the output voltage is .....
(*i*) 180° out of phase with the input
(*ii*) in phase with the input
(*iii*) 90° out of phase with the input
(*iv*) taken at the source

46. In a certain common-source *D-MOSFET* amplifier, $V_{ds} = 3.2$ V r.m.s. and $V_{gs} = 280$ mV r.m.s. The voltage gain is .....
(*i*) 1 (*ii*) 11.4
(*iii*) 8.75 (*iv*) 3.2

47. In a certain *CS JFET* amplifier, $R_D = 1$ kΩ, $R_S = 560$Ω, $V_{DD} = 10$ V and $g_m = 4500$ μS. If the source resistor is completely bypassed, the voltage gain is .....
(*i*) 450 (*ii*) 45
(*iii*) 2.52 (*iv*) 4.5

48. A certain common-source *JFET* has a voltage gain of 10. If the source bypass capacitor is removed, ...
(*i*) the voltage gain will increase
(*ii*) the transconductance will increase
(*iii*) the voltage gain will decrease
(*iv*) the Q-point will shift

49. A *CS JFET* amplifier has a load resistance of 10 kΩ and $R_D = 820$Ω. If $g_m = 5$ mS and $V_{in} = 500$ mV, the output signal voltage is ...
(*i*) 2.05 V (*ii*) 25 V
(*iii*) 0.5 V (*iv*) 1.89 V

50. If load resistance in Q. 49 is removed, the output voltage will .....
(*i*) increase (*ii*) decrease
(*iii*) stay the same (*iv*) be zero

Answers to Multiple-Choice Questions

1. (*iii*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*ii*)	**5.** (*i*)
6. (*iii*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*iv*)
11. (*iii*)	**12.** (*ii*)	**13.** (*i*)	**14.** (*iii*)	**15.** (*ii*)
16. (*i*)	**17.** (*ii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*iii*)
21. (*ii*)	**22.** (*i*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*i*)	**28.** (*iv*)	**29.** (*ii*)	**30.** (*i*)
31. (*iv*)	**32.** (*iii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*i*)
36. (*ii*)	**37.** (*iii*)	**38.** (*i*)	**39.** (*iv*)	**40.** (*ii*)
41. (*iii*)	**42.** (*i*)	**43.** (*ii*)	**44.** (*i*)	**45.** (*i*)
46. (*ii*)	**47.** (*iv*)	**48.** (*iii*)	**49.** (*iv*)	**50.** (*i*)

Chapter Review Topics

1. Explain the construction and working of a *JFET*.
2. What is the difference between a *JFET* and a bipolar transistor ?
3. How will you determine the drain characteristics of *JFET* ? What do they indicate?
4. Define the *JFET* parameters and establish the relationship between them.
5. Briefly describe some practical applications of *JFET*.
6. Explain the construction and working of *MOSFET*.
7. Write short notes on the following :
   (*i*) Advantages of *JFET* (*ii*) Difference between *MOSFET* and *JFET*

Problems

1. A *JFET* has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS(off)}$ is – 6 V, find the value of (*i*) V_{GS} and (*ii*) V_P. **[(*i*) – 1.5 V (*ii*) 6 V]**
2. A *JFET* has an I_{DSS} of 9 mA and a $V_{GS\,(off)}$ of – 3V. Find the value of drain current when V_{GS} = –1.5V. **[2.25mA]**
3. In the *JFET* circuit shown in Fig. 19.64 if I_D = 1.9 mA, find V_{GS} and V_{DS}. **[– 1.56V; 13.5V]**

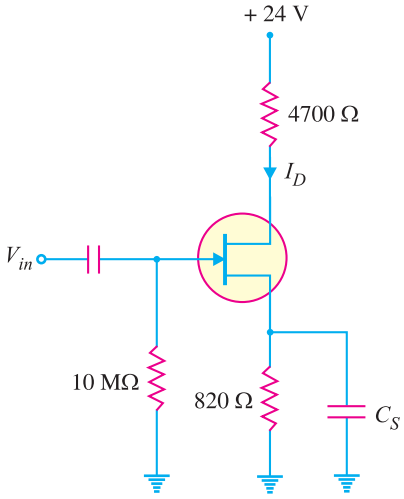


Fig. 19.64

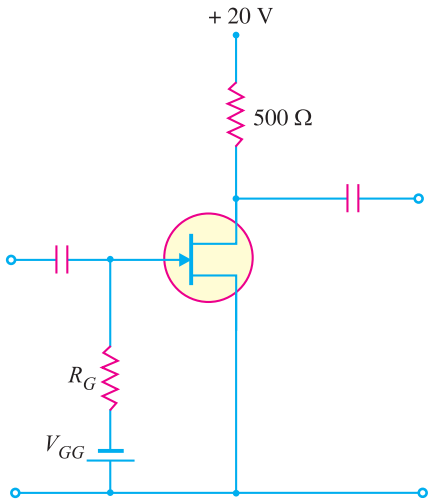


Fig. 19.65

4. For the *JFET* amplifier shown in Fig. 19.65, draw the d.c. load line.

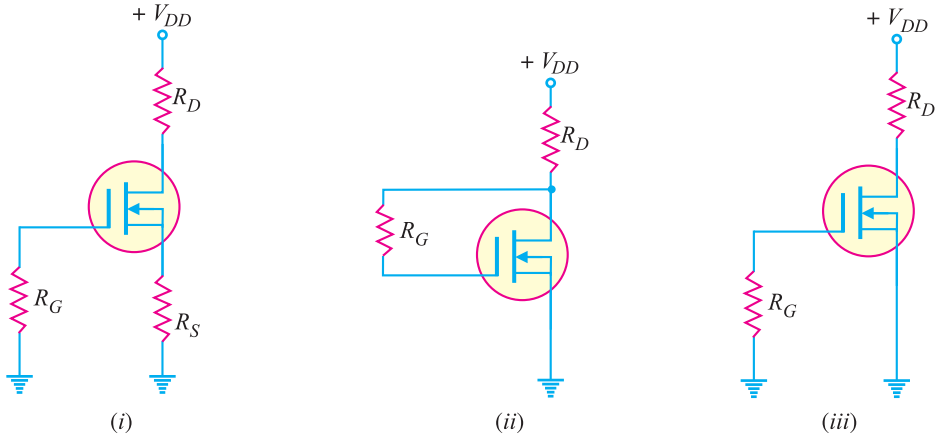


Fig. 19.66

5. For a *JFET*, $I_{DSS} = 9$ mA and $V_{GS} = -3.5$ V. Determine I_D when (*i*) $V_{GS} = 0$ V (*ii*) $V_{GS} = -2$V.
[(*i*) 9mA (*ii*) 1.65 mA]
6. Sketch the transfer curve for a *p*-channel *JFET* with $I_{DSS} = 4$ mA and $V_P = 3$ V.
7. In a *D-MOSFET*, determine I_{DSS}, given $I_D = 3$ mA, $V_{GS} = -2$V and $V_{GS\,(off)} = -10$V. **[4.69 mA]**
8. Determine in which mode each *D-MOSFET* in Fig. 19.66 is biased.
[(*i*) Depletion (*ii*) Enhancement (*iii*) Zero bias]
9. Determine V_{DS} for each circuit in Fig. 19.67. Given $I_{DSS} = 8$ mA. **[(*i*) 4V (*ii*) 5.4V (*iii*) – 4.52V]**

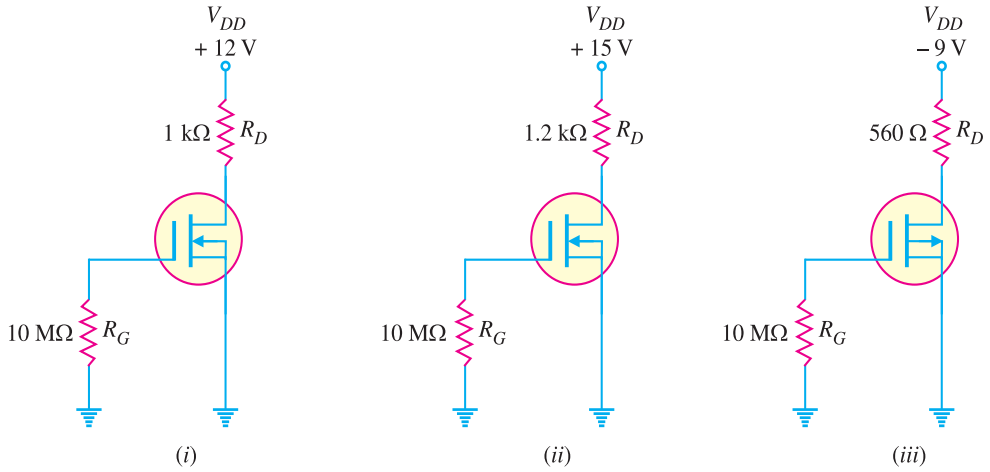


Fig. 19.67

10. If a 50 mV r.m.s. input signal is applied to the amplifier in Fig. 19.68, what is the peak-to-peak output voltage? Given that $g_m = 5000$ µS. **[920 mV]**

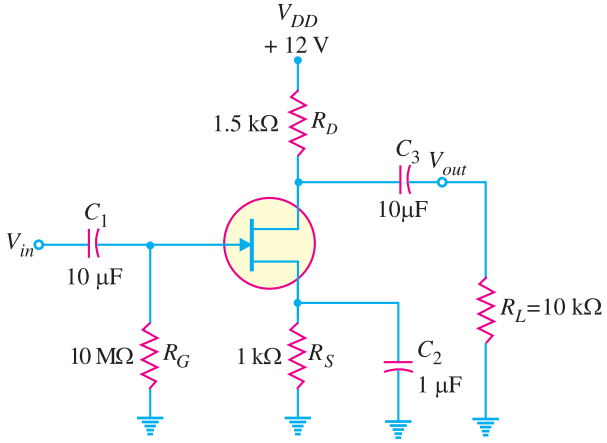


Fig. 19.68

Discussion Questions

1. Why is the input impedance of *JFET* more than that of the transistor ?
2. What is the importance of *JFET* ?
3. Why is *JFET* called unipolar transistor ?
4. What is the basic difference between *D-MOSFET* and *E-MOSFET* ?
5. What was the need to develop *MOSFET* ?

Top

Fig. 31.23

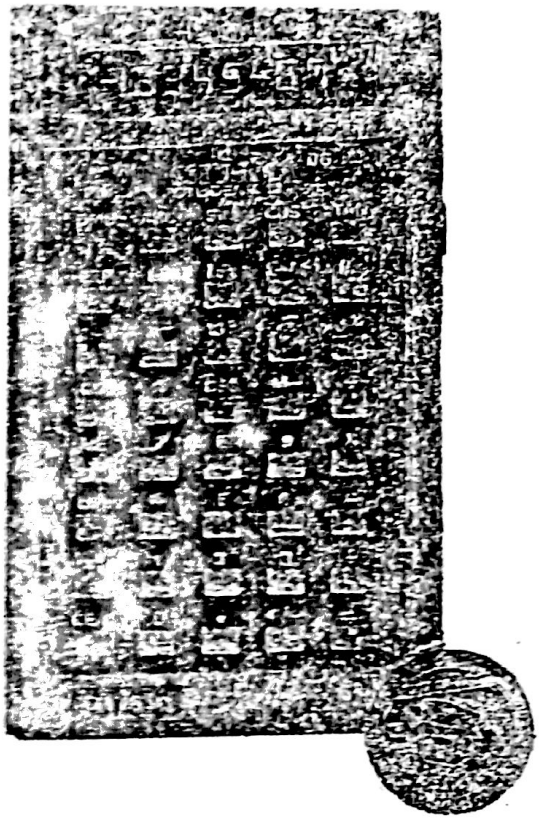


Fig. 31.24

2. There is no need for isolation technique for enhancement MOSFET devices since each source and drain region is isolated from the other by the P-N junctions formed within the N-type substrate. This fact is shown in Fig. 31.25 where two P-channel E-MOSFETs have been fabricated from the same substrate.

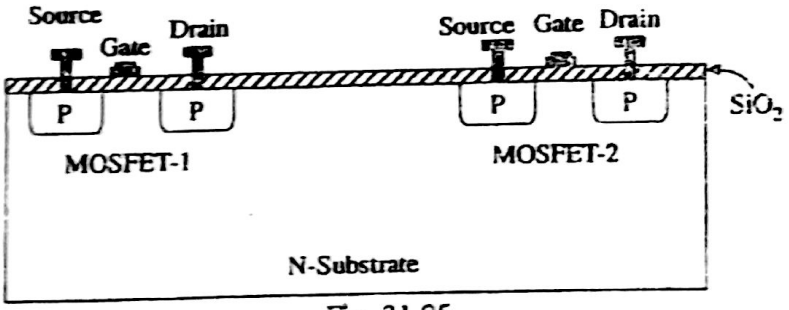


Fig. 31.25

3. The packing density of MOS ICs is at least ten times more than that for bipolar ICs. Also, a MOS resistor occupies less than 1 per cent of the area of a conventional diffused resistor. This high packing density makes MOS ICs especially suited for LSI and VLSI.

The main disadvantage of MOS ICs is *their slower operating speed as compared to bipolar ICs*. Hence, they do not compete with bipolar ICs in ultrahigh-speed applications.

However, due to their (*i*) low cost (*ii*) low power consumption and (*iii*) high packing density, MOS ICs are widely used for LSI and VLSI chips such as calculator chips, memory chips and microprocessors (μP).

31.18. What is an OP-AMP ?

It is a very high-gain, high-r_{in} directly-coupled negative-feedback amplifier which can amplify signals having frequency ranging from **0 Hz to a little beyond 1 MHz.** They are made with different internal configurations in linear ICs. An OP-AMP is so named because it was originally designed to perform mathematical operations like summation, subtraction, multiplication, differentiation and integration etc., in analog computers. Present day usage is much wider in scope but the popular name OP-AMP continues.

Typical uses of OP-AMP are : scale changing, analog computer operations, in instrumentation

and control systems and a great variety of phase-shift and oscillator circuits. The OP-AMP is available in three different packages (*i*) standard dual-in-line package (DIP) (*ii*) TO-5 case and (*iii*) the flat-pack.

Although an OP-AMP is a complete amplifier, it is so designed that external components (resistors, capacitors etc.) can be connected to its terminals to change its external characteristics. Hence, it is relatively easy to tailor this amplifier to fit a particular application and it is, in fact, due to this versatility that OP-AMPs have become so popular in industry.

An OP-AMP IC may contain two dozen transistors, a dozen resistors and one or two capacitors.

Example of OP-AMPs

1. μA 709—is a high-gain operational amplifier constructed on a single silicon chip using planar epitaxial process.
   It is intended for use in dc servo systems, high-impedance analog computers and in low-level instrumentation applications.
   It is manufactured by Semiconductors Limited, Pune.
2. [LM 108 – LM 208]— Manufactured by Semiconductors Ltd., Mumbai.
3. CA 741 CT and CA 741 T—these are high-gain operational amplifiers which are intended for use as (*i*) comparator, (*ii*) integrator, (*iii*) differentiator, (*iv*) summer, (*v*) dc amplifier, (*vi*) multivibrator, and (*vii*) bandpass filter.
   Manufactured by Bharat Electronics Ltd. (BEL), Bangalore.

31.19. OP-AMP Symbol

Standard triangular symbol for an OP-AMP is shown in Fig. 31.26 (*a*) though the one shown in Fig. 31.26 (*b*) is also used often. In Fig. 31.26 (*b*), **the common ground line has been omitted.** It also does not show other necessary connections such as for dc power and feedback etc.

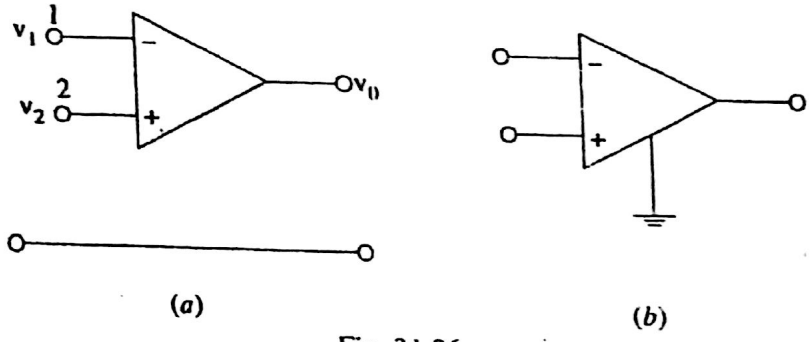


Fig. 31.26

The OP-AMP's input can be single-ended or double-ended (or differential input) depending on whether input voltage is applied to one input terminal only or to both. Similarly, amplifier's output can also be either single-ended or double-ended. The most common configuration is *two input terminals and a single output.*

All OP-AMPs have a minimum of five terminals

1. inverting input terminal,
2. non-inverting input terminal,
3. output terminal,
4. positive bias supply terminal,
5. negative bias supply terminal.

31.20. Polarity Conventions

In Fig. 31.26 (*b*), the input terminals have been marked with minus (–) and plus (+) signs. These are meant to **indicate the inverting and non-inverting terminals only** [Fig. 31.27 (*a*)]. It simply means that a signal applied at negative input terminal will appear amplified but **phase-inverted at the output terminal** as shown in Fig. 31.27 (*b*). Similarly, signal applied at the positive input terminal will appear amplified and **in-phase** at the output. Obviously, these plus and minus polarities **indicate phase reversal only**. It does not mean that voltage v_1 and v_2 in Fig. 31.27 (*a*) are negative and positive respectively. Additionally, it also does not imply that

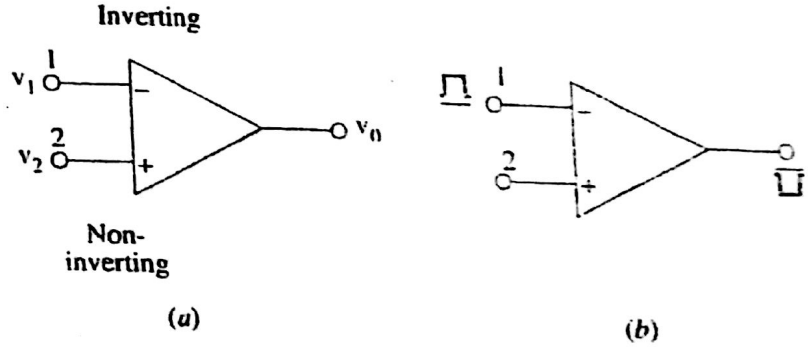


Fig. 31.27

positive input voltage has to be connected to the plus-marked non-inverting terminal 2 and negative input voltage to the negative-marked inverting terminal 1. In fact, the amplifier can be used 'either way up' so to speak. It may also be noted that all input and output voltages are referred to a common reference usually the ground shown in Fig. 31.26 (*a*).

1.21. Ideal Operational Amplifier

When an OP-AMP is operated without connecting any resistor or capacitor from its output to any one of its inputs (*i.e.*, without feedback), it is said to be in the **open-loop condition**. The word 'open loop' means that *feedback path or loop is open*. The specifications of an OP-AMP under such condition are called open-loop specifications.

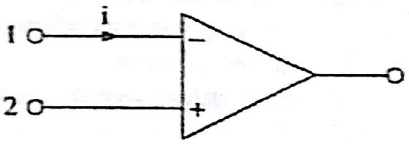
An ideal OP-AMP (Fig. 31.28) has the following characteristics:

1. its open-loop gain A_v is *infinite i.e.*, $A_v = -\infty$;
2. its input resistance R_i (measured between inverting and non-inverting terminals) is *infinite i.e.*, $R_i = \infty$ ohm;
3. its output resistance R_0 (seen looking back into output terminals) is *zero i.e.*, $R_0 = 0\ \Omega$;
4. it has *infinite bandwidth i.e.*, it has flat frequency response from dc to infinity.

Though these characteristics cannot be achieved in practice, yet an ideal OP-AMP serves as convenient reference against which real OP-AMPs may be evaluated.

Following additional points are worth noting:

1. Infinite input resistance means that input current $i = 0$ as indicated in Fig. 31.28.
   It means that an ideal OP-AMP is a voltage-controlled device.
2. $R_o = 0$ means that v_o is not dependent on the load resistance connected across the output.
3. Though for an ideal OP-AMP $A_v = \infty$, for an actual one, it is extremely high *i.e.*, about 10^6. However, it does not mean that 1 V signal will be amplified to 10^6 V at the output. Actually, the maximum value of v_0 is limited by the bias supply voltage, typically ± 15 V. With $A_v = 10^6$ and $v_0 = 15\ V_2$ the maximum value of input voltage is limited to $15/10^6 = 15\ \mu V$. Though 1 V cannot become 1 million volt in the OP-AMP, 1 μV can certainly become 1 V.



$A_v = -\infty$
$R_i = \infty$
$BW = \infty$
$R_o = 0$
$i = 0$

Fig. 31.28

31.22. Virtual Ground and Summing Point

In Fig. 31.29 is shown an OP-AMP which employs *negative feedback* with the help of resistor R_f which feeds a portion of the output to the input.

Since input and feedback currents are algebraically added at point *A*, it is called the **summing point.**

The concept of **virtual** ground arises from the fact that input voltage v_i at the inverting terminal of the OP-AMP is forced to such a small value that, for all practical purposes, it may be assumed to be zero. Hence, point *A* is essentially at ground voltage and is referred to as *virtual ground*. Obviously, *it is not the actual ground*, which, as seen from Fig. 31.29, is situated below.

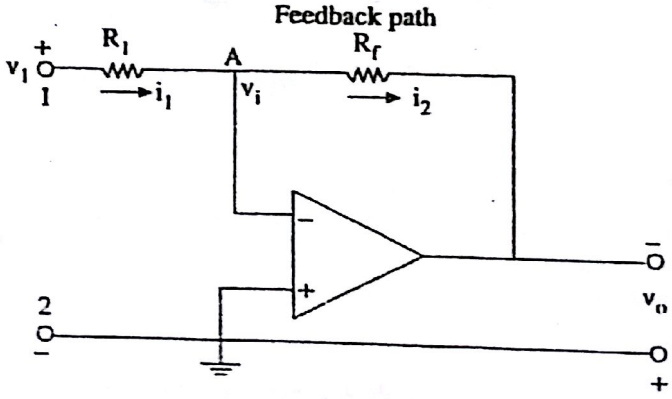


Fig. 31.29

31.23. Why V_i is Reduced to almost Zero ?

When v_1 is applied, point *A* attains some positive potential and at the same time v_o is brought into existence. Due to negative feedback, some fraction of the output voltage is fed back to point *A* antiphase with the voltage already existing there (due to v_1).

The algebraic sum of the two voltages is almost zero so that $v_i = 0$. Obviously, v_i will become exactly zero when **negative feedback voltage at A is exactly equal to the positive voltage produced by v_1 at A.**

Another point worth considering is that there exists a virtual short between the two terminals of the OP-AMP because $v_i = 0$. It is virtual because no current flows (remember $i = 0$) despite the existence of this short.

31.24. OP-AMP Applications

We will consider the following applications:

1. as scaler or linear (*i.e.*, small-signal) constant-gain amplifier; both inverting and non-inverting
2. as unity follower,
3. Adder or Summer,
4. Subtractor,
5. Integrator,
6. Differentiator,
7. Comparator.

Now, we will discuss the above circuits one by one assuming an ideal OP-AMP.

31.25. Linear Amplifier

We will consider the functioning of an OP-AMP as a constant-gain amplifier both in the inverting and non-inverting configurations.

(*a*) Inverting Amplifier or Negative Scale

As shown in Fig. 31.30, non-inverting terminal has been grounded whereas R_1 connects the input signal v_1 to the inverting input. A feedback resistor R_f has been connected from the output to the inverting input.

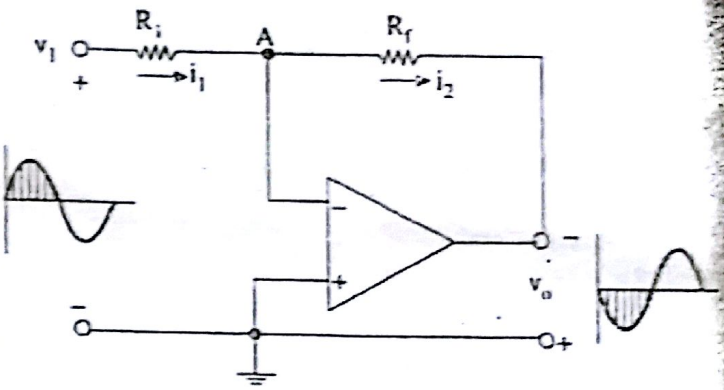


Fig. 31.30

Gain

Since point A is at ground potential*, $i_1 = \dfrac{v_{in}}{R_1} = \dfrac{v_1}{R_1}$

$$i_2 = \frac{-v_o}{R_f}$$ — please note – ve sign

Using KCL (Art. 3.2) for point A,

$$i_1 - (-i_2) = 0 \quad \text{or} \quad \frac{v_1}{R_1} + \frac{v_o}{R_f} = 0 \quad \text{or} \quad \frac{v_0}{R_f} - \frac{v_1}{R_1} \text{ or } \frac{v_0}{v_1} = -\frac{R_f}{R_1}$$

$$\therefore \quad A_v = -\frac{R_f}{R_1} \text{ or } A_v = -K \qquad \text{Also,} \quad v_o = -Kv_{in}$$

It is seen from above, that closed-loop gain of the inverting amplifier depends on the ratio of the two external resistors R_1 and R_f and is independent of the amplifier parameters.

It is also seen that the OP-AMP works as a negative scaler. It scales the input *i.e.*, it multiplies the input by a minus constant factor K.

(*b*) Non-inverting Amplifier or Positive Scaler

This circuit is used when there is need for an output which is equal to the input multiplied by a positive constant. Such a positive scaler circuit which uses negative feedback but provides an output that equals the input multiplied by a positive constant is shown in Fig. 31.31.

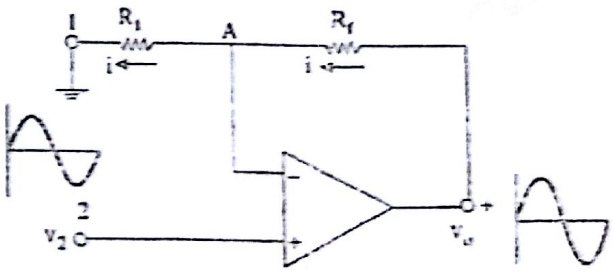


Fig. 31.31

* If not, then $i_1 = \dfrac{v_1 - v_i}{R_1}$ and $i_2 = \dfrac{v_0 - v_1}{R_f}$.

Since input voltage v_2 is applied to the non-inverting terminal, the circuit is also ... non-inverting amplifier.

Here, polarity of v_o is the same as that of v_2 *i.e.*, both are positive.

Gain

Because of virtual short between the two OP-AMP terminals, voltage across R_1 is the input voltage v_2. Also, v_0 is applied across the series combination of R_1 and R_f

$$\therefore \quad v_{in} = v_2 = iR_1 ; \qquad v_0 = i(R_1 + R_f)$$

$$\therefore \quad A_v = \frac{v_o}{v_{in}} = \frac{i(R_1 + R_f)}{iR_1} \qquad \text{or} \qquad A_v = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

Alternative Derivation

As shown in Fig. 31.32, let the currents through the two resistors be i_1 and i_2.

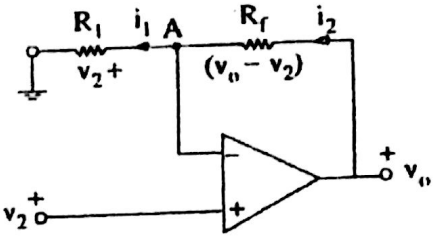


Fig. 31.32

The voltage across R_1 is v_2 and that across R_f is $(v_o - v_2)$.

$$\therefore \quad i_1 = \frac{v_2}{R_1} \qquad \text{and} \qquad i_2 = \frac{v_o - v_2}{R_f}$$

Applying KCL to junction A, we have

$$(-i_1) + i_2 = 0 \qquad \text{or} \qquad \frac{-v_2}{R_1} + \frac{(v_o - v_2)}{R_f} = 0$$

$$\therefore \quad \frac{v_o}{R_f} = v_2\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = v_2\frac{R_1 + R_f}{R_1 R_f}$$

$$\therefore \quad \frac{v_o}{v_2} = \frac{R_1 + R_f}{R_1} \qquad \text{or} \quad A_v = 1 + \frac{R_f}{R_1} \qquad \text{—as before}$$

Example 31.1. *Calculate (i) input impedance and (ii) the voltage gain of the OP-AMP amplifier circuit of Fig. 31.33.*

Solution. (*i*) The input impedance of the OP-AMP amplifier is very high and when negative feedback is used, the impedance is increased even further. Hence, input impedance of a non-inverting OP-AMP amplifier can be thought of as infinite.

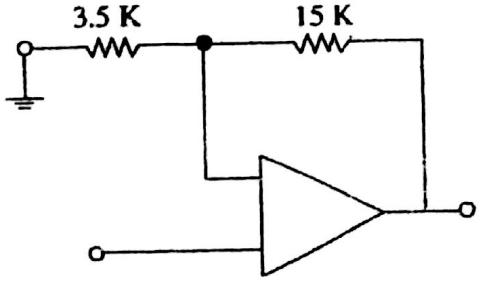


Fig. 31.33

(*ii*) The voltage gain is given by

$$A_v = 1 + \frac{R_f}{R_1} = 1 + \frac{15}{3.5} = \mathbf{5.3}$$

Example 31.2. *For the inverting amplifier of Fig. 31.30, $R_1 = 1K$ and $R_f = 1M$. Assuming an ideal OP-AMP amplifier, determine the following circuit values :*

(a) voltage gain, (b) input resistance , (c) output resistance.

Solution. It should be noted that we will be calculating values *of the circuit* and not *for the* OP-AMP *proper.*

(*a*) $A_v = -\dfrac{R_f}{R_1} = -\dfrac{1000\text{ K}}{1\text{ K}} = \mathbf{-1000.}$

(*b*) Because of virtual ground at A, $R_{in} = R_1 = \mathbf{1\text{ K}}$.

(*c*) Output resistance of the circuit equals the output resistance of the OP-AMP *i.e.*, **zero ohm.**

31.26. Unity Follower

It provides a gain of unity without any phase reversal. It is very much similar to the emitter follower (Art. 21.8) except that its gain is very much closer to being exactly unity.

This circuit (Fig. 31.34) is useful as a buffer or isolation amplifier because it allows input voltage v_{in} to be transferred as output voltage v_o while at the same time preventing load resistance

R_L from loading down the input source. It is due to the fact that its $R_i = \infty$ and $R_o = 0$.

In fact, circuit of Fig. 31.34 can be obtained from that of Fig. 31.31 by putting

$$R_1 = R_f = 0$$

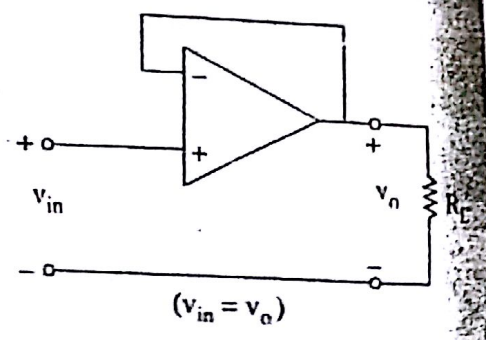


Fig. 31.34

31.27. Adder or Summer

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. It is basically similar to a scaler (Fig. 31.30) except that it has more than one input. Fig. 31.35 shows a three-input inverting adder circuit. As seen, *the output voltage is phase-inverted.*

Calculations

As before, we will treat point A as virtual ground

$$i_1 = \frac{v_1}{R_1} \quad \text{and} \quad i_2 = \frac{v_2}{R_2}$$

$$i_3 = \frac{v_3}{R_3} \quad \text{and} \quad i = -\frac{v_o}{R_f}$$

Applying KCL to point A, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or $$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} - \left(\frac{-v_o}{R_f}\right) = 0$$

$$\therefore \quad v_o = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$$

or $$v_o = -(K_1 v_1 + K_2 v_2 + K_3 v_3)$$

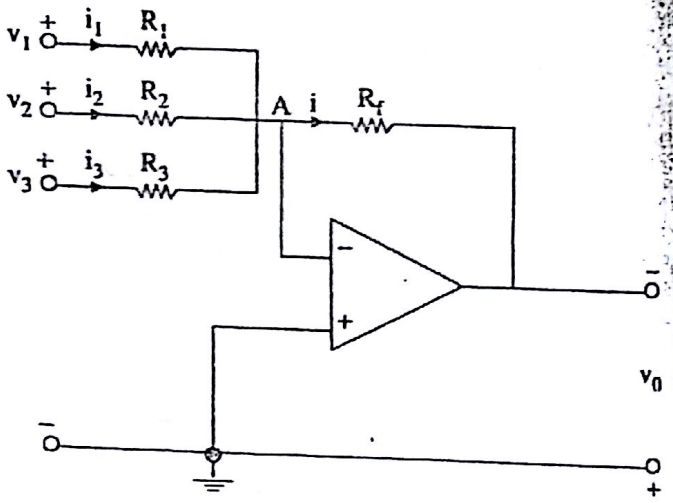


Fig. 31.35

The overall negative sign is unavoidable because we are using the inverting input terminal.

If $R_1 = R_2 = R_3 = R$, then

$$v_o = -\frac{R_f}{R}(v_1 + v_2 + v_3) = -K(v_1 + v_2 + v_3)$$

Hence, output voltage is proportional to (*not equal to*) the **algebraic sum** of the three input voltages.

If $R_f = R$, then output exactly equals the sum of inputs. However, if $R_f = R/3$,

then $$v_o = -\frac{R/3}{R}(v_1 + v_2 + v_3) = -\frac{1}{3}(v_1 + v_2 + v_3)$$

Obviously, the output is equal *to the average of the three inputs.*

31.28. Subtractor

The function of a subtractor is to provide an output proportional to or equal to the difference of two input signals. As shown in Fig. 31.36, we have to apply the inputs at the inverting as well as non-inverting terminals.

Calculations

According to Superposition Theorem (Art. 4.2)

$$v_o = v_o' + v_o''$$

where v_o' is the output produced by v_1 and v_o'' is that produced by v_2.

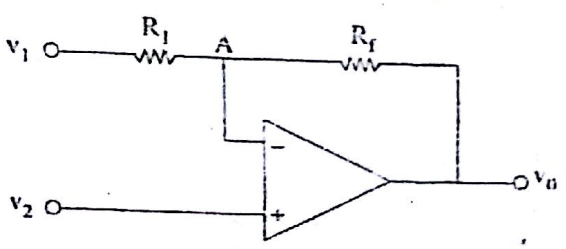


Fig. 31.36

Now, $v_o' = -\frac{R_f}{R_1} \cdot v_1$ — Art. 31.25 (*a*)

$$v_o'' = \left(1 + \frac{R_f}{R_1}\right) v_2$$ — Art. 31.26 (*b*)

$$\therefore \quad v_o = \left(1 + \frac{R_f}{R_1}\right) v_2 - \frac{R_f}{R_1} v_1$$

Since $R_f \gg R_1$ and $R_f / R_1 \gg 1$, hence

$$v_o \equiv \frac{R_f}{R_1}(v_2 - v_1) = K(v_2 - v_1)$$

Further, if $R_f = R_1$, then

$v_o = (v_2 - v_1)$ = difference of the two input voltages.

Obviously, if $R_f \neq R_1$, then a scale factor is introduced.

Example 31.3. *Find the output voltage of an OP-AMP inverting adder for the following sets of input voltages and resistors. In all cases, $R_f = 1M$.*

$$v_1 = -3\ V, v_2 = +3\ V. v_3 = +2\ V;\ R_1 = 250\ K,\ R_2 = 500\ K, R_3 = 1\ M$$

Solution. $v_o = -(K_1 v_1 + K_2 v_2 + K_3 v_3)$

$$K_1 = \frac{R_f}{R_1} = \frac{1000\ K}{250\ K} = 4,\ K_2 = \frac{1000}{500} = 2,\ K_3 = \frac{1\ M}{1\ M} = 1$$

$$\therefore \quad v_o = -[(4 \times -3) + (2 \times 3) + (1 \times 2)] = +4\ \mathbf{V}$$

Example 31.4. *In the subtractor circuit of Fig. 31.36, $R_1 = 5\ K$, $R_f = 10\ K$, $v_1 = 4\ V$ and $v_2 = 5\ V$. Find the value of output voltage.*

Solution. $v_o = \left(1 + \frac{R_f}{R_1}\right) v_1 - \frac{R_f}{R_1} v_2 = \left(1 + \frac{10}{5}\right) 4 - \frac{10}{5} \times 5 = +2\ \mathbf{V}$

31.29. Integrator

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage.

A simple example of integration is shown in Fig. 31.37 where input is dc level and its integral is *a linearly-increasing ramp output.*

The actual integrating circuit is shown in Fig. 31.38. This circuit is similar to the scaler circuit of Fig. 31.29 except that **the feedback component is a capacitor C instead of a resistor R_f.**

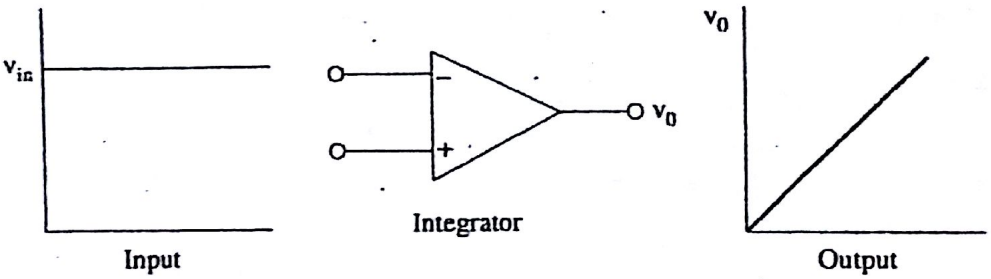


Fig. 31.37

Calculations

As before, point A will be treated as virtual ground.

$$i_1 = \frac{v_1}{R};\quad i_2 = -\frac{v_o}{X_C} = -\frac{v_o}{1/j\omega C} = -\frac{v_o}{1/sC} = -sC\,v_o$$

where $s = j\omega$ in the Laplace notation.

Now $i_1 = i_2$ — Art. 31.20 (*a*)

$$\therefore \quad \frac{v_1}{R} = -sCv_o$$

$$\therefore \quad \frac{v_o}{v_{in}} = \frac{v_o}{v_1} = -\frac{1}{sCR}$$

$$\therefore \quad A_v = -\frac{1}{sCR}$$

Now, the expression of Eq. (*i*) can be written in time domain as

$$v_o(t) = -\frac{1}{CR}\int v_1(t)\ .\ dt$$

It is seen from above that output (right-hand side expressions) is an integral of the input, with an inversion and a scale factor of $1/CR$.

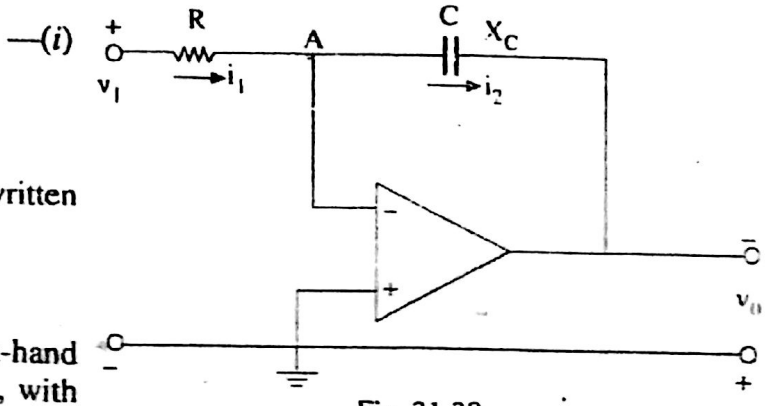


Fig. 31.38

This ability to integrate a given signal enables an analog computer to solve differential equations and to set up a wide variety of electrical circuit analogs of physical system operations. For example, let

$R = 1$ M and $C = 1\ \mu$F. Then

$$\text{scale factor} = -\frac{1}{CR} = -\frac{1}{10^6 \times 10^{-6}} = -1$$

As shown in Fig. 31.39, the input is a step voltage whereas output is a ramp (or linearly-changing voltage) with a scale multiplier of –1.

However, when $R = 100$ K, then

$$\text{scale factor} = -\frac{1}{10^5 \times 10^{-6}} = -10$$

$$\therefore \quad v_0(t) = -10\int v_1(t).\,dt$$

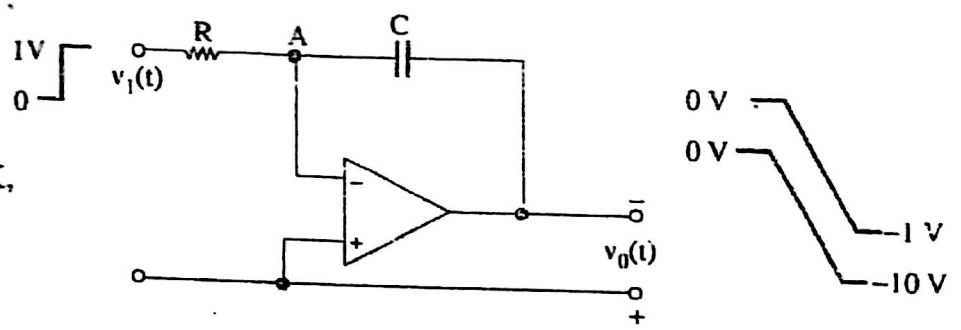


Fig. 31.39

It is also shown in Fig. 31.39. Of course, we can integrate more than one input as shown below in Fig. 31.40. With multiple inputs, the output is given by

$$v_o(t) = -[K_1\int v_1(t)\,dt + K_2\int v_2(t)\,dt + K_3\int v_3(t)\,dt]$$

where $K_1 = \frac{1}{CR_1}$, $K_2 = \frac{1}{CR_2}$ and $K_3 = \frac{1}{CR_3}$

Fig. 31.40 (*a*) shows a summing integrator as used in an analog computer. It shows all the three resistors and the capacitor. The analog computer representation of Fig. 31.40 (*b*) indicates only the scale factor for each input.

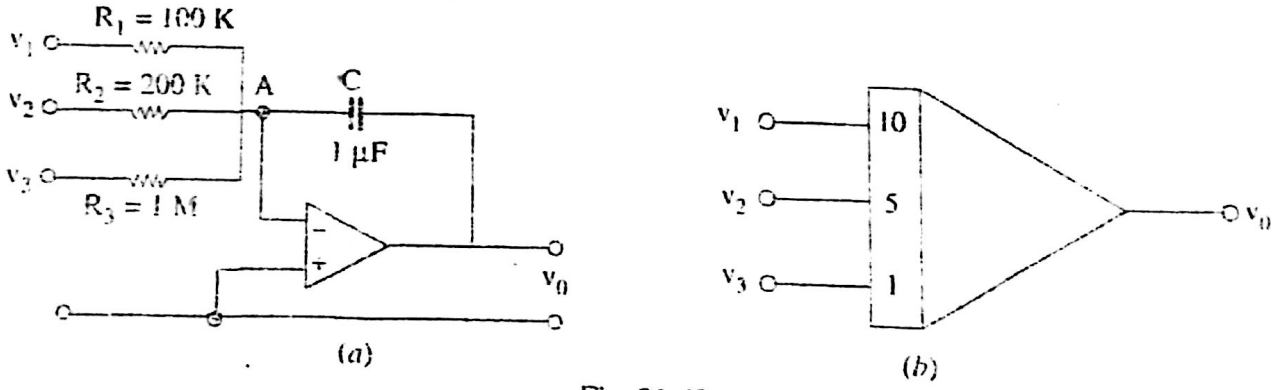


Fig. 31.40

Example 31.5. *A 5 mV, 1 kHz sinusoidal signal is applied to the input of an OP-AMP integrator of Fig. 31.38 for which R = 100 K and C = 1 μF. Find the output voltage.*

tion. Scale factor $= -\frac{1}{CR} = \frac{1}{10^5 \times 10^{-6}} = -10$

The equation for the sinusoidal voltage is

$$v_i = 5 \sin 2\pi f t = 5 \sin 2000\pi t$$

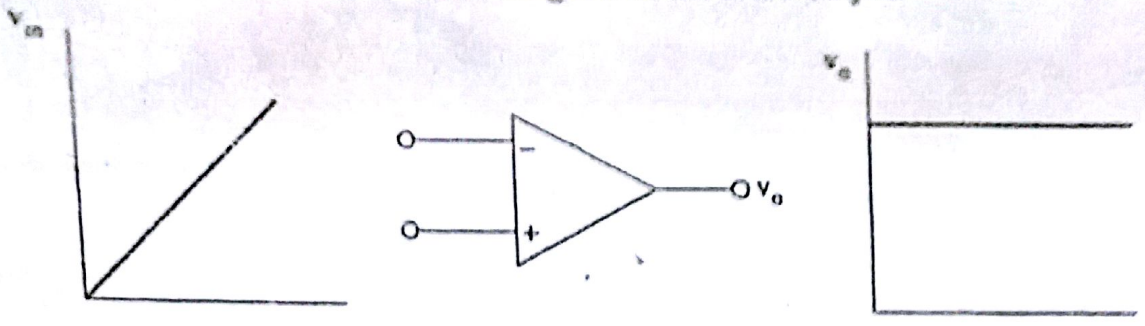
Obviously, it has been assumed that at $t = 0$, $v_i = 0$

$$\therefore \quad v_0(t) = -10 \int_0^t 5 \sin 2000\pi t = -50 \left| \frac{-\cos 2000\pi t}{2000} \right|_0^t$$

$$= \frac{1}{40\pi} (\cos 2000\pi t - 1)$$

31.30. Differentiator

Its function is to provide an output voltage which *is proportional to the rate of change of the input voltage.* It is an inverse mathematical operation to that of an integrator. As shown in Fig. 31.41, when we feed a differentiator, we get a constant dc output.



Input Differentiator Output

Fig. 31.41

Circuit

Differentiator circuit can be obtained *by interchanging the resistor and capacitor of the integrator circuit of Fig. 31.38.*

Let i = rate of change of charge $= \frac{dq}{dt}$

Now, $q = Cv_c$

$$\therefore \quad i = \frac{d}{dt}(Cv_c) = C \frac{dv_c}{dt}$$

Taking point A as virtual ground

$$v_o = -iR = -\left(C \cdot \frac{dv_c}{dt}\right) R$$

$$= -CR \cdot \frac{dv_c}{dt}$$

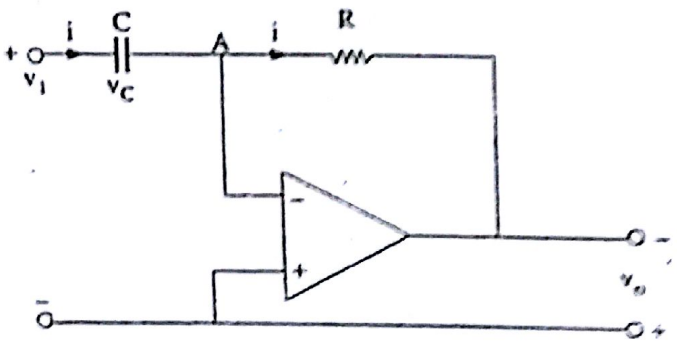


Fig. 31.42

As seen, output voltage is proportional to the derivate of the input voltage, the constant of proportionality (*i.e.*, scale factor) being $(-CR)$.

Example 31.7. *The input to the differentiator circuit of Fig. 31.42 is a sinusoidal voltage of peak value 5 mV and frequency 1 kHz. Find out the output if $R = 100$ K and $C = 1$ μF.*

Solution. The equation of the input voltage is

$$v_i = 5 \sin 2\pi \times 1000t = 5 \sin 2000\pi t \text{ mV}$$

scale factor $= CR = 10^{-6} \times 10^5 = 0.1$

$$v_0 = 0.1 \frac{d}{dt}(5 \sin 2000\pi t) = (0.5 \times 2000\pi) \cos 2000\pi t$$

$$= 1000\pi \cos 2000\pi t \text{ mV}$$

As seen, output is a cosinusoidal voltage of frequency 1 kHz and peak value 1000π mV.